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-: HAND WRITTEN NOTES:-

OF

ELECTRONICS & COMMUNICATION ENGINEERING

-: SUBJECT:-

ELECTRONIC DEVICES & CIRCUITS

1

THERMAL VOLTAGE :→ (V_T) :→

"Volt equivalent of temp"

$$\Rightarrow \boxed{V_T = \frac{\bar{K}T}{q} \text{ volts}}$$

T = Temp. in kelvin

q = charge → 1.6×10^{-19} C.

$\bar{K}$ = Boltzmann constt. → 1.381×10^{-23} J/°K.

K = 8.62×10^{-5} eV/°K.

$$\Rightarrow \boxed{V_T = \frac{T}{11600} \text{ volt}}$$

$$\Rightarrow \boxed{V_T \propto T}$$

if T = 0K, $V_T = 0$

⇒ T = 300K, V_T = 26 mV

$$\left[\therefore V_T = \frac{300}{11600} = 26\text{mV} \right]$$

* For a large variation in temperature there will be small variation in thermal voltage.

Temp. in °C = Temp. in kelvin − 273

T = 0K ⇒ −273°C (Absolute temp)

T = 300K ⇒ 27°C (Room temp).

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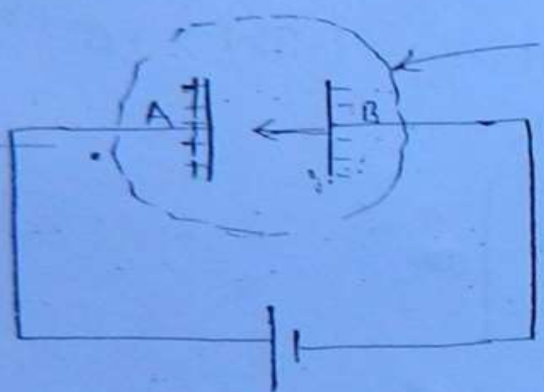
Temp. in kelvin = °C + 273

→ Electron volt (eV) :→

→ It is the practical unit for energy in electronics

→ 1 eV is defined as the energy gain by electron is moving to a potential difference of 1 volt



$$1\ eV = |q| \times P_d$$

$$= 1.6 \times 10^{-19} C \times 1\ volt$$

$$1\ eV = 1.6 \times 10^{-19}\ C\text{-}volt\ /\ Joule$$

$$\Rightarrow 1\ eV = 1.6 \times 10^{-19}\ J$$

$K.E. = \frac{1}{2}mv^2$, $P.E. = qV$

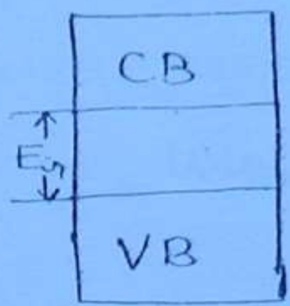
eV indicates the kinetic energy gain by electron or potential energy lost by electron

K.E. gain = P.E. lost

$$\frac{1}{2}mv^2 = qV \Rightarrow \underset{\text{velocity}}{v} = \sqrt{\frac{2.q.V}{m}} \Rightarrow v = \sqrt{\frac{2qV}{m}}$$

$m = 9.1 \times 10^{-31}$ kg metre / sec

Energy Gap → E_G or E_g ⇒



Also called Band gap or Forbidden energy band.

	Ge	Si
E_{G0} =	0.785 eV	1.21 eV
E_{G300} =	0.72 eV	1.1 eV

$$\Rightarrow \quad E_G \propto \frac{1}{\text{Temperature}}$$

⇒ In semiconductors and insulators, energy gap decreases with the temperature increases.

$$\Rightarrow \quad E_{G(T)} = (E_{G0} - \beta_0 T)\ eV$$

β_0 → material constant → eV/°K

For Si

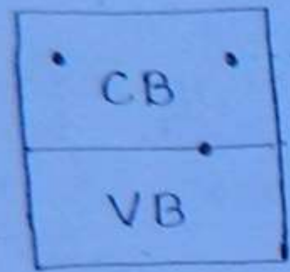
$$\Rightarrow \quad E_{G(T)} = (1.21 - 3.6 \times 10^{-4}\,T)\ eV$$

For Ge

$$\Rightarrow \quad E_{G(T)} = (0.785 - 2.2 \times 10^{-4}\,T)\ eV$$

(i) Energy band diagram for metal or conductors :-

⇒ For metal $E_g = 0$ at $T = 0K$

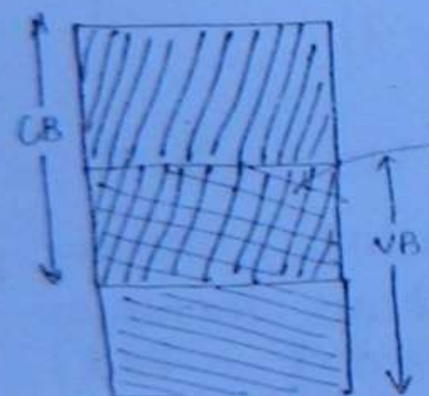


e^- (free e^- available)

at T=0K

In metal free e^- conc^n is available at 0 K.

At T= 300K



overlapping of VB & CB

⇒ Overlap ∝ Temperature

density or conc^n of e^- $(n) = 10^{28}/m^3$ in metal

⇒ metals possesses metallic bonding.

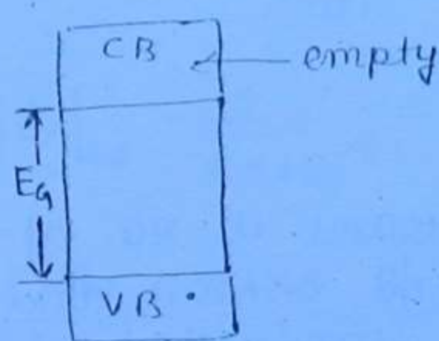
⇒ Due to overlapping of VB & CB, metals will exhibit positive temperature coefficient of resistance (PTC)

⇒ Free e^- conc^n in the metal is almost independent of temperature.

⇒ In metal electron concentration : $n = 10^{28}/m^3$ which is highly concentrated electron.

(ii) <u>Energy band Diagram for Insulators</u> :→

$E_G \rightarrow$ large $\geq 5\,eV$.



⇒ All insulators are bad conductors of current i.e. they do not allow any flow of current through them.

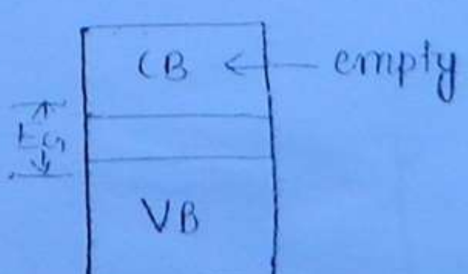
⇒ <u>Ionic bonding</u> occurs in insulator.

<u>e.g.</u> Air, diamond, <u>Mica</u>, Ceramic, glass, paper, wood, SiO_2; Rubber, <u>Bakelite</u>, <u>PVC</u>, cloth <u>Porcelain</u>.

(iii) <u>Energy band diagram for semiconductor</u> :→

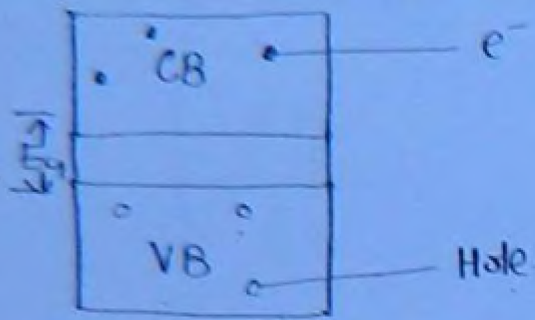
$E_G \rightarrow$ small $\rightarrow$ around $1\,eV$
↳ $0.7\,eV$ to $1.3\,eV$

at T = 0K



→ All semiconductors are insulator at 0K.

At T = 300K



⇒ When temperature increases a no. of covalent bond will be broken and electron and holes are created and therefore a conductivity in semiconductor.

eg Silicon and Germanium.

Semiconductors are the elements whose conductivity lies inbetween the conductivity of a insulator and the conductivity of a conductor of a conductor.

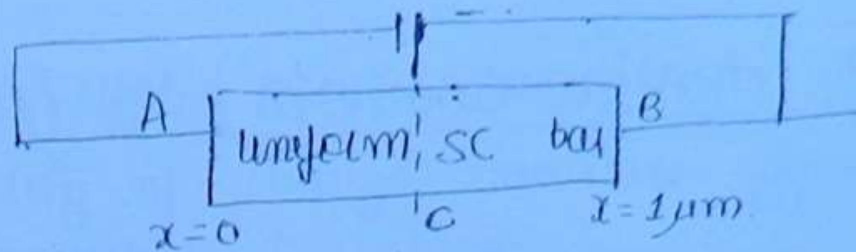
Electric field Intensity ($\mathcal{E}$ or E)

or field intensity
or field gradient
or field

$$\Rightarrow \quad \mathcal{E} = -\frac{dv}{dx} \quad V/m$$

$$\Rightarrow \quad |\mathcal{E}| = \frac{\text{Voltage existing}}{\text{spacing or distance}}$$

Prob



|E| at point B

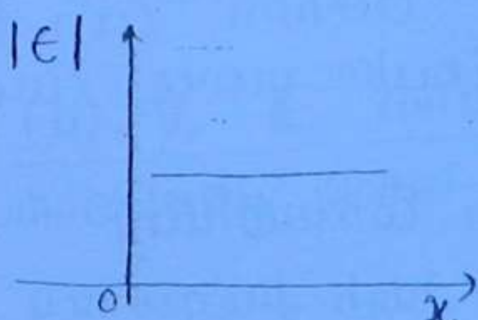
$$|\epsilon| = \frac{|V_B|}{x_{at\,B}}$$

$$|\epsilon|_{at\,B} = \frac{1}{1\times10^{-6}} = \underline{10^6\ V/m}$$

|E| at the centre of bar

$$|\epsilon|_{at\,C} = \frac{0.5\ V}{0.5\,\mu m} = \underline{10^6\ V/m}$$

⇒ On a uniform semiconductor bar field intensity will remain a constant throughout the semiconductor bar except at x=0 (not defined).



MOBILITY of charge carriers $\Rightarrow (\mu)$

mobility is defined as

$$\mu = \frac{\text{Drift Velocity}}{\text{Field Intensity}} = \frac{v}{\epsilon} = \frac{m}{s} \times \frac{m}{V} = m^2/V\text{-sec}$$

⇒ Mobility indicates how fast the charge carrier will be moving from one place to another place.

	Ge	Si
electron mobility (μ_n) =	3800 $cm^2/V\text{-sec}$	1300 $cm^2/V\text{-sec}$
Hole mobility (μ_p) =	1800 $cm^2/V\text{-sec}$	500 $cm^2/V\text{-sec}$

Ge: $\frac{\mu_n}{\mu_p} = 2.1 : 1$, Si: $\frac{\mu_n}{\mu_p} = 2.6 : 1$

⇒ Electron mobility is always greater than hole mobility and therefore electron can travel faster and also contributes more current than a hole.

⇒ Ge
- → Higher conductivity
- → used for high frequency becoz of high product gain bandwidth [more suitable than Si]

⇒ Switching time are very small and therefore Si is more suitable for switching applications

⇒ Si : High power handling.

⇒ mobility of charge carriers decreases with the temperature.

⇒ As temperature is increasing the atom in the material will be vibrating and due to this thermal vibration it causes the mobility of charge carriers decreases.

$$\boxed{\mu \propto T^{-m}}$$

where m is material constant

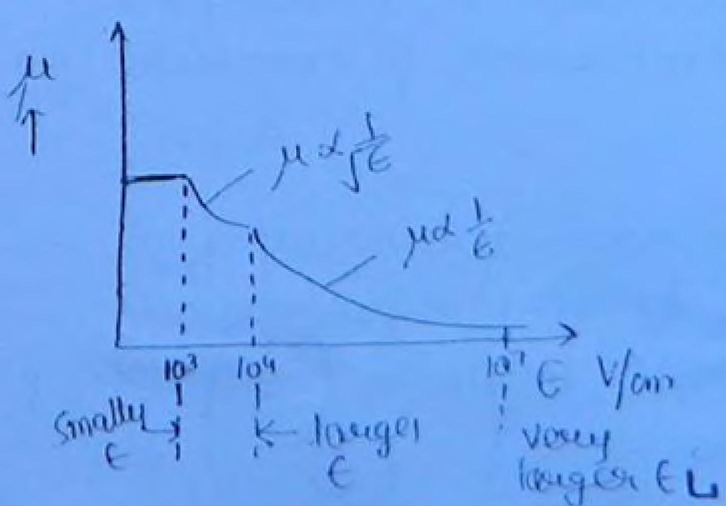
For Ge → 1.66 for e^-
2.33 for hole

Si → 2.5 for e^-
2.7 for hole

} only for IES.

⇒ mobility decreases with the temperature as a non-linear variation.

⇒ Mobility (μ) Vs $\mathcal{E}$ curve or graph → {Only for IES
(experimentally plotted graph)



⇒ Drift velocity $v = \mu E$

⇒ For smaller field intensity is applying (10^3) or $< 10^3$

(i) Mobility of charge carrier will remain constant.

(ii) Drift velocity will be linearly increasing with field intensity.

⇒ For larger field intensity is applying ($> 10^7$) ⇒

(i) Mobility of charge carriers decreases

(ii) Drift velocity will remain almost a constant. Drift velocity will enters into saturation.

⇒ In a semiconductor the field intensity is gradually increasing :→ The drift velocity ⇒

(i) linearly increases

(ii) Sublinearly increases

(iii) enters into saturation for larger field applied

END OF DAY 80

Current :→

Current is defined as rate of change of charge

$$\Rightarrow \boxed{i = \frac{dq}{dt}} \text{ Amphere}$$

⇒ In the semiconductor current is carried by both electrons and holes.

Drift current :→

It is the flow of current to the material or device under the influence of electric field intensity.

Temperature Coefficient (TC) ⇒

- NTC (Negative TC)
- PTC (positive TC).

NTC :→ Any parameter decreasing with the temperature is called NTC

e.g. Resistance of semiconductor or insulator. E_G, μ.

PTC :→ Any parameter increasing with the temperature is called PTC.

e.g Resistance of metal, V_T, I_o (likeage current

Einsteins Equation.

In a SC

$$\Rightarrow \frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = V_T$$

$$\Rightarrow \frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{T}{11600}$$

* $$\Rightarrow \frac{\mu_n}{D_n} = \frac{\mu_p}{D_p} = \frac{1}{V_T} = \frac{11600}{T}$$

[∵ D_n and D_p are diffusion constt of e^- & holes resp.]

⇒ It gives the relationship between diffusion constt, mobility and thermal voltage.

* $\frac{D}{\mu} \propto$ Temp.

  $\frac{\mu}{D} \propto \frac{1}{\text{Temp}}$

* The unit of mobility to Diffusion constt is V^{-1} ✓

* The unit of D/μ is Volts ✓

Diffusion constant of charge carrier (D) :→

e^- Diffusion constt. $D_n = \mu_n V_T$

Hole " ———— $D_p = \mu_p V_T$

Unit for Diffusion constant $\frac{cm^2}{V\text{-}sec} \times V = $ m^2/sec or cm^2/sec

⇒ It is a material constant and is responsible for the property called diffusion in the semiconductors.

⇒ Diffusion constt decreases with the temperature

For Ge at 300K

$D_n = \mu V_T = 3800 \times 2.6 \times 10^{-1}$

$D_n = 99\ cm^2/s$.

$D_p = 47\ cm^2/s$

For Si at 300k.

$D_n = 34\ cm^2/s$

$D_p = 13\ cm^2/s$

→ Diffusion constant cannot be negative and also it cannot be fraction.

Mass Action law.

$$\Rightarrow \boxed{np = n_i^2} \Rightarrow [\text{other then IES exam}]$$

In a semiconductor (intrinsic or extrinsic) under thermal equillbrium. The product of electrons and holes in the semiconductor will be always a constant and is equal to the square of intrinsic concentration. (n_i).

$\Rightarrow$ The law is mainly used for extrinsic semiconductor to calculate the minority carrier concentration.

N-type SC

Majority carriers are $e^- \Rightarrow n_n$

Minority carrier are holes $\Rightarrow p_n$

$$\Rightarrow \boxed{p_n = \frac{n_i^2}{n_n}}$$

P-type semiconductor.

Majority carriers are holes $\Rightarrow p_p$

Minority carriers are $e^- \Rightarrow n_p$

$$\Rightarrow \boxed{n_p = \frac{n_i^2}{p_p}}$$

→ In a semiconductor :→

⇒ $n_n P_n = n_i^2$

⇒ $n_p P_p = n_i^2$

⇒ $np = n_n P_n = n_i^2$

$np = n_p P_p = n_i^2$

⇒ Minority carrier concⁿ $= \dfrac{n_i^2}{\text{majority carrier conc}^n}$

⇒ Majority carrier concⁿ ∝ Doping concⁿ ☆

⇒ Minority carrier concⁿ $\propto \dfrac{1}{\text{Doping conc}^n}$ ☆

INTRINSIC CONCⁿ (n_i) :→

$n = p = n_i$

⇒ Intrinsic concⁿ (n_i) → it is concⁿ available in pure semiconductor at a given temp.

⇒ n_i indicates electron or hole concⁿ for per unit volume for at a given temp.

$$\Rightarrow \boxed{n_i^2 = A_0 T^3 e^{-E_{G0}/KT}}$$

Replacing E_{G0} by E_G.

$$\Rightarrow \boxed{n_i^2 = A_0 T^3 e^{-E_G/KT}}$$

$\therefore A_0 \rightarrow$ material constant

$$\Rightarrow \begin{cases} n_i^2 \propto T^3 & \rightarrow \text{dominating more} \\ n_i^2 \propto e^{-E_G/KT} & \rightarrow E_G \text{ dominating less} \end{cases}$$

⇒ Intrinsic concⁿ depends on :-

1. Temperature
2. Energy gap.

Intrinsic concⁿ $n_i \propto \boxed{T^{3/2}}$

Intrinsic concⁿ $n_i^2 \propto \boxed{T^3}$

⇒ Becoz of smaller E_G Ge is having larger value of n_i then compare to Si.

For Ge n_i :→ $n_i = 2.5 \times 10^{13}$ atoms/cm³

For Si n_i :→ $n_i = 1.5 \times 10^{10}$ atoms/cm³

Resistivity (ρ) :⇒ or Specific resistance of the material.

unit of $\rho \rightarrow \Omega$-m or Ω-cm or S.

For metals: ⇒

PTC of Resistance

R ↑ with T ↑

$$\left[\because \rho = \frac{Rl}{A}\right]$$

⇒ **ρ ↑ with T ↑**

For SC. ⇒

NTC of Resistance

⇒ R ↓ with T ↑

ρ ↓ with T ↑

Conductivity (σ) :→

It is the reciprocal of ~~reciproicit~~ ~~resistan~~ resistivity.

unit of σ → $\frac{1}{\Omega m}$ or Ω^{-1}/m = $\mho/m$

or $\mho/m$

⇒ Conductivity denotes current carrying capacity of material or device.

⇒ **Conductivity = Carrier concⁿ × charge × mobility**

⇒ Conductivity depends on :→
(1) carrier concⁿ
(2) Mobility of charge carriers
(3) charge

For metal
↓
unipolar

⇒ $\sigma = nq\mu_n$ Ω^{-1}/m

⇒ $\sigma \downarrow$ with $T \uparrow$

⇒ In metals as temp. is increasing, mobility of charge carrier decreases and therefore conductivity of metal decreases.

⇒ In metals free e^- conc^n is independent of temperature.

For SC.
↓
Bipolar

⇒ $\boxed{\sigma = nq\mu_n + pq\mu_p}$ Ω^{-1}/cm.

⇒ $\boxed{\sigma \uparrow \text{ with Temp} \uparrow}$

⇒ When temperature is increasing, mobility of charge carrier decreases it will slightly reduce the conductivity. that but at the same time becoz of thermal energy a large no of covalent bond will be broken and e^- and holes are created and this will increase the conductivity by a larger value and the net result in the semiconductor conductivity increases with the temperature.

⇒ In a semiconductor conductivity mainly depends on carrier concentration.

Current Density (J) :→

It is the current passing per unit area.

$$J = \frac{I}{Area} \Rightarrow Amp/m^2$$

$$J = \sigma E \quad Amp/cm^2$$

Current density in metal :→

$$\Rightarrow J = nq\mu_n E_0$$

For semiconductor.

$$\Rightarrow J = [nq\mu_n + pq\mu_p] E_0 \quad Amp/cm^2$$

Electrical properties of Ge and Si

Properties	Ge	Si
1) Atomic No. →	32	14
2) Total No. of atom or density →	4.421×10^{22}	5×10^{22}
3) Intrinsic concⁿ (n_i) at 300K atoms/cm^3 →	2.5×10^{13}	1.5×10^{10}
4) Intrinsic resistivity (ρ_i) (Ω-cm) →	45	2,30,000.
5) Leakage current (I_0) →	μA	nA
6) Maximum operating temp. →	75°C	175°C
7) Power handling capability →	Low	High

⇒ Silicon is more fancy when compare to germanium and this is due to :→

(1) Smallest likeage current.
(2) High temperature application.
(3) High power handling.
(4) Abundance on surface of earth.
(This is primary reason why Si is more fancy buy semiconductor device manufacture
(5) Low cost.
(6) Suitable to modify into SiO_2.
⇓
[This is the main reason why Si is very much fancy by IC manufacturers.]

Disadvantages of Si

⇒ main disadvantages is conductivity is less.

⇒ why carbon is not considered as semiconductor material ?

IV group → C, Si, Ge.

⇒ C belongs to fourth group of periodic table but $E_G > 1.5\ eV$

⇒ The properties of C are highly unstable, unreliable and unpredictable properties.

⇒ C sometimes will behaves as conductor eg Graphite
Sometimes it behaves as insulator e.g. Diamond

⇒ Due to this reason C never consider as a SC element.

MAXIMUM Operating Temperature

For Ge,

−60° C to +75° C

⇒ Max operating temp. = 75°C.

For Si.

−60°C to 175°C.

⇒ max operating temp. = 175°C.

⇒ **Normal working Temperature**

⇒ **100 K to 400 K**.

Gallium Arsenide (GaAs)

Ga → 3rd group; As → 5th group

- Direct band gap SC
- ⇒ $E_G = 1.47\ eV$

- $\mu_n = 5600$ to $85 \cdot cm^2/V\text{-}s$
- $\mu_p = 400\ cm^2/V\text{-}sec$

⇒ GaAs is artificially make with Ga fro 3rd group & Arsenic from 5th group

⇒ Highly expensive material

⇒ Best e.g of Direct Band gap SC.

⇒ During the Recombination energy will b dissipated in the form of light

⇒ The Best microwave material.

⇒ GaAs exhibits negative Differential mobility & due to this property it is more suitab[le for] microwave application

⇒ GaAs is low noise material. ($\frac{1}{f}$ noise)↓

⇒ GaAs is used in the fabrication LED's, tunnel diode, varactor diode, pin diode, impatt diode gunn diode, microwave IC.

⇒ InP (Indium Phosphate) is used In place of GaAs Nowadays

Leakage current (I_o) :→

	Ge	Si
$I_o =$	μA	nA

I_o of Ge > I_o of Si

{For 1°C ↑ by approx. 7%

★ {I_o doubles for every 10°C}}

⇒ Also called minority carrier current or reverse saturation current or Thermally generated current.

⇒ For the better performance of the material or device likeage current must be smaller. So that the temperature effect on the material will be less.

⇒ Si is having better thermal stability than Ge

⇒ I_o is independent of applied voltage i.e. this current is saturated in respect to the applied voltage.

⇒ I_o depends on the no. of minority carriers and minority carrier concⁿ depends on temp.

⇒ I_o is highly sensitive to temperature

⇒ $$I_{o(T_2)} = I_{o(T_1)} \left[2^{T_2 - T_1/10} \right] \text{ Amp}$$

where $T_2 > T_1$

Diffusion and Diffusion Current

⇒ Diffusion is a natural phenomena

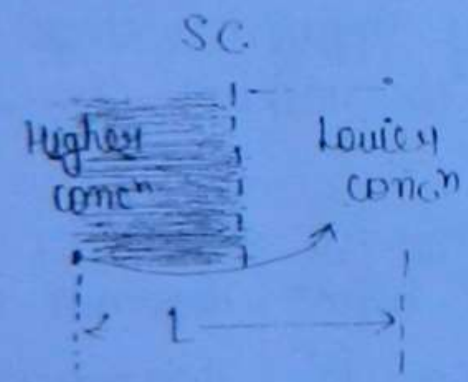
⇒ The migration of charge carriers of higher concⁿ to lower concⁿ or from higher density to lower density is called Diffusion

⇒ Diffusion current flows only in semiconductors

⇒ In a semiconductor diffusion is mainly due to concentration gradient

⇒ In a semiconductor diffusion is due to unequal distribution of charge carriers.

⇒ Diffusion is also associated with random motion of charge carriers due to thermal vibrations.



gradient → $\frac{d}{dx}$

$\frac{dn}{dx}$ → e^- concⁿ gradient

$\frac{dp}{dx}$ → hole concⁿ gradient

Length of Diffusion $L = \sqrt{D \cdot \tau}$ (m)

D → Diffusion constt of charge carrier.

τ → carrier lifetime

↳ Average lifetime of e^- or hole.

☆ { Length of Diffusion refers to average length.

∴ $D = \mu V_T$

⇒ ⇒ $L = \sqrt{\mu V_T \cdot \tau}$

⇒ length of diffusion depends on

(1) Diffusion constt of charge carrier.

(2) Temperature

(3) carrier lifetime

(4) Mobility of charge carrier.

e^- Diffusion current Density $J_{n(diff)}$

☆ $J_{n(diff)} = +q D_n \frac{dn}{dx}$ A/cm^2 for gate exam problem

Hole diffusion current density $J_{p(diff)}$

☆ $J_{p(diff)} = -q D_p \frac{dp}{dx}$ A/cm^2

⇒ In the above equation q is : charge and its value is taken in magnitude (1.6×10^{-19} C).

⇒ <u>e^- diffusion current</u> $(I_{n(diff.)}) = J_{n(diff.)} \times A$

⇒ hole diffusion current $(I_{p(diff.)}) = J_{p(diff.)} \times A$.

{∴ if A is not given take $A = 1$ }
while solving problem.

Total Current Density in a semiconductor

⇒ The total current density (J)

⇒ $$J = J_n + J_p \quad A/cm^2$$

where $J_n = J_{n(Drift)} + J_{n(Diff)}$

⟹ $$J_n = nq\mu_n E + q D_n \frac{dn}{dx}$$

where $J_p = J_{p(Drift)} + J_{p(Diff.)}$

$$= nq\mu_p E + (-q) D_p \frac{dp}{dx}$$

⇒ $$J_p = pq\mu_p E - q D_p \frac{dp}{dx}$$

Prob: If the Drift velocity of holes under a field gradient of 100 V/m is 5 m/sec what is mobility?

Ans:
$$\mu = \frac{v}{E} = \frac{5}{100} = 0.05\ m^2/V\text{-sec}$$

Prob. The carrier mobility in a semiconductor is 0.4 m^2/V-sec. Its diffusion constt. at 300K will be ____ .

Soln
$$D = \mu V_T$$
$$= 0.4 \times 26 \times 10^{-3}$$
$$= 0.0104\ m^2/s$$

Prob. The minority carrier lifetime and diffusion constt in a semiconductor material are 100 μs and 100 cm^2/s. resp. Diffusion length of charge carriers ____ .

Soln
$$L = \sqrt{D \cdot \tau}$$
$$L = \sqrt{100 \times 10^{-6} \times 100}$$
$$\boxed{L = 10^{-1}\ cm}$$

Prob. A sample of n-type SC has e^- density of $6.25 \times 10^{18}/cm^3$ at 300 K. If intrinsic concn of charge carrier in sample is $2.5 \times 10^{13}/cm^3$ find hole concn.

Soln
$$P_n = \frac{n_i^2}{n_n} = \frac{(2.5 \times 10^{13})^2}{6.25 \times 10^{18}} = 10^8/cm^3$$

Prob A flat Al strip with a resistivity of $3.44 \times 10^{-8}\ \Omega$-m and length 5mm and a cross sectional area 2×10^{-4} mm² find the voltage drop across the strip when a current of 50mA is passing through it.

Solⁿ

$$V = IR$$

$$R = \frac{\rho L}{A} = \frac{3.44 \times 10^{-8} \times 10^{3} \times 5}{2 \times 10^{-4}}$$

$$R = \frac{\overset{1.72}{\cancel{3.44}} \times 10^{-1} \times 5}{\cancel{2}} = = .86\ \Omega$$

$$V = IR$$

$$V = 50 \times .86$$

$$\boxed{V = 43\ mV}$$

Prob A SC wafer is 0.5mm thick a potential of 100 mV is applied at across thickness

→ what is the e^- drift velocity. if the mobility is $0.2\ m^2/V$-sec.

→ How much time is reqd. for an e^- to move across this thickness.

Solⁿ

$$\mu = \frac{v}{E} \Rightarrow \mu = \frac{v}{V/l} = 0.2 \quad \frac{v}{\frac{100 \times 10^{-3}}{0.5 \times 10^{-3}}}\ (200)$$

$$v = 200 \times 0.2 = 40\ m/s$$

Time taken by e^- $= \frac{0.5 \times 10^{-3}}{40} = \boxed{12.5\ \mu sec}$

Prob A small concⁿ of minority carriers is injected into a homogeneous SC ~~resistor~~ crystal at one point and having an electric field of 10 V/cm is applied across the ~~syst~~ crystal so that minority carriers in that crystal will be moving at distance of 1 cm in 20 μs. calculate mobility in $cm^2/V\text{-}sec$.

Soln

$\epsilon = 10\ V/cm$

$dx = 1\ cm$

$\mu = \frac{v}{\epsilon}$

$\Rightarrow \epsilon = \frac{V}{L} \Rightarrow 10 = \frac{V}{1} = \boxed{V = 10V}$

~~[illegible]~~

$$\text{Drift velocity} = \frac{\text{Distance}}{\text{Time}}$$

$$= \frac{1\ cm}{20 \times 10^{-6}\ sec} = 50,000\ cm/s$$

$$\mu = \frac{v}{\epsilon} = \frac{50,000}{10} = 5000\ cm^2/sec.$$

Prob In Ge the likeage currents are 5μA at 10°c find its value in the temperature is 25°c.

Soln

$$I_{o(T_2)} = I_{o(T_1)} \left[2^{\frac{T_2 - T_1}{10}} \right]$$

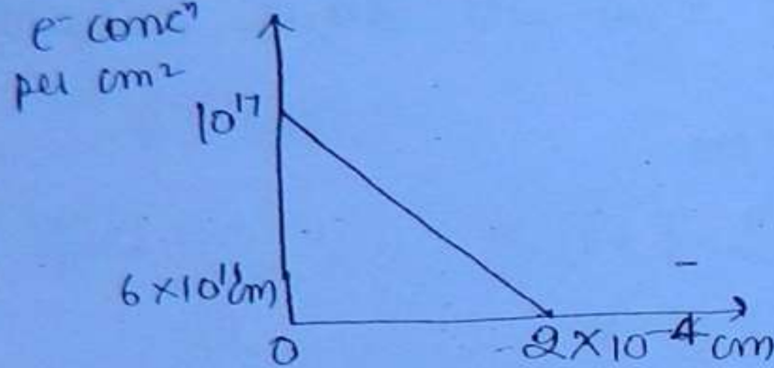
$$= 5\mu A \left[2^{\frac{25-10}{10}} \right].$$

$$= 14.14\ \mu A$$

workbook problem

(20) : done e 10^{17}/cm³

Soln



e^- current density = $J_{n(diff.)} + J_{n(drift)}$

since $E = 0$ (given)

$\therefore J_{n(drift)} = 0$

$J_n = J_{n(diff.)}$

$= +q D_n \frac{dn}{dx}$

$= 1.6 \times 10^{-19} \times 35 \left[\frac{6 \times 10^{16} - 10^{17}}{2 \times 10^{-4} - 0}\right]$

Ans (B) $= -1120$ A/cm²

INTRINSIC SEMICONDUCTOR.

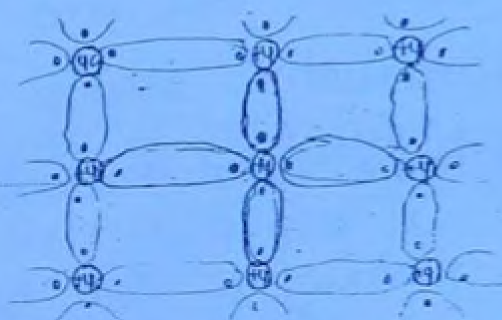
or Pure SC.
or Non-degenerated SC.

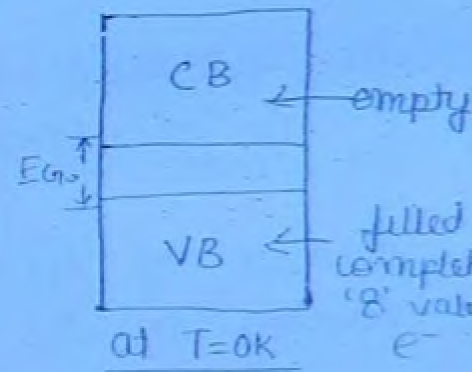
⇒ The maximum valency e^- in the atom is 8.

⇒ semiconductor exhibit the property of covalent bonding.

Crystalline structure.

at T=0K



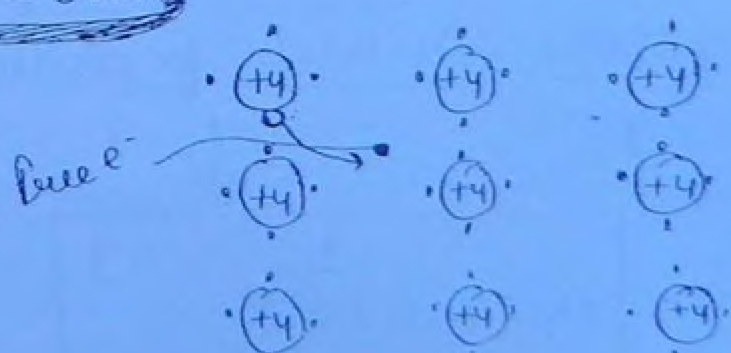


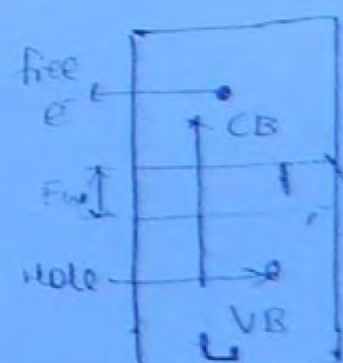
⇒ The sharing of e^- with the neighbouring atom is called covalent Bonding.

⇒ In one covalent bonding there will be two e^- at 0K, All valency e^- are in perfect covalent bonding and therefore the valency band is completely filled.

⇒ Intrinsic semiconductor at 0K will behave as perfect insulator.

At T=300K





⇒ [n=p]

⇒ When a covalent bond is broken it will create one e^- and one hole (e^- will be jumping from VB to CB and becomes a free e^- and hole will remain in VB)

⇒ Hole is defined as defficiency of e^- in the broken covalent bond.

⇒ Hole is a carrier of current with a +ve charge of $+1.6 \times 10^{-19}$ C.

⇒ In intrinsic semiconductor always $\boxed{n = p}$

⇒ The cond^n for intrinsic semiconductor $\boxed{n = p = n_i}$

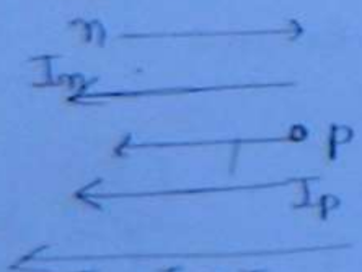
⇒ Because of opposite polarity e^- and hole will be moving in the opposite direction.

⇒ Current direction is opposite to the flow of e^-

⇒ Current direction is in direction hole flow.

⇒ <u>In a SC</u>

<u>Left</u> <u>Right</u>



$I = I_n + I_p$

but $I_n > I_p$

e^- and hole will be always moving in the opposite direcⁿ but they contribute the current in the same direction.

The free e^- will be moving in the conduction band and will contribute some current but at the same time hole will be moving in VB but in the opposite direction and will contribute some current and the total current 'I' is the sum of e^- current and hole current

The conductivity of intrinsic semiconductor is

$$\sigma_i = nq\mu_n + pq\mu_p \ \mho/cm$$

but $n = p = n_i$

$$\Rightarrow \boxed{\sigma_i = n_i q[\mu_n + \mu_p]} \ \mho/cm$$

$$\sigma_i \propto n_i$$

but $n_i \propto T^{3/2}$

$$\sigma_i \propto T^{3/2} \text{ (approx.)}$$

$$\boxed{\sigma_i \uparrow \quad T \uparrow}$$ As a Non-linear variation

The resistivity of intrinsic semiconductor

$$\rho = \frac{1}{\sigma_i}$$

$$\Rightarrow \boxed{\rho = \frac{1}{n_i q(\mu_n + \mu_p)}}$$

(i) Disadvantages of Intrinsic SC. :→

⇒ conductivity is very small.

(ii) Generation of e^- hole pair :→

⇒ When temperature is increasing covalent bonds will be broken creating e^- and holes. and this process is called generation of e^- hole pair.

(iii) Recombination. :→

⇒ The free e^- pairing with hole is called Recombination

⇒ During the recombination the free e^- and the hole will disappear and a covalent bond is created

⇒ During the Recombination the free e^- will be falling from conduction band to valence band to recombine with the hole and the energy is dissipated in the form of heat and light.

(iv) Carrier lifetime (τ) :→

⇒ It is the interval of time from breaking of covalent bond until its recombination.

⇒ Carrier lifetime is average lifetime.

⇒ τ is μ sec to n sec measured.

⇒ Hole is a valency e⁻ but taken with a positive charge.

Prob Calculate intrinsic conductivity and intrinsic resistivity of Ge at room temp. assume $n_i = 2.5 \times 10^{13}$ atom/cm³. $\mu_n = 3800$ cm²/v-sec

$\mu_p = 1800$

soln

$$\sigma_i = n_i q (\mu_p + \mu_n)$$

$$\sigma_i = 2.5 \times 10^{13} \times 1.6 \times 10^{-19} (3800 + 1800)$$

$$\sigma_i = 2.5 \times 10^{-6} \times 5600 \times 1.6$$

$$\sigma_i = 2.5 \times 56 \times 10^{-4} \times 1.6$$

$$\sigma_i = 140.0 \times 10^{-4} \times 1.6$$

$$\sigma_i = 140 \times 10^{-4} = 1.4 \times 10^{-2} \times 1.6$$

$$\Rightarrow \sigma_i = 0.0224 \ \Omega^{-1}/cm$$

$$\Rightarrow \rho_i = \frac{1}{0.0224} = 44.6 \ \Omega\text{-cm}$$

Prob Calculate conductivity & resistivity of pure Si at room temp. assume $n_i = 1.5 \times 10^{10}$/cm³

$\mu_n = 1300$ & $\mu_p = 500$

soln

$$\sigma_P = 1.5 \times 10^{10} \times 1.6 \times 10^{-19} (1800)$$

$$\sigma_i = 1.5 \times 1.6 \times 18 \times 10^{-7}$$

$$\sigma_i = 2.40 \times 18 \times 10^{-7} = 4.32 \times 10^{-6} \ \mho/cm$$

$$\rho_i = \frac{1}{\sigma_i} = \boxed{231,481 \ \Omega\text{-cm}}$$

Conductivity variation in the semiconductor with temp.

⇒ In intrinsic semiconductor conductivity will increases with temperature.

For 1°C, In Ge $\sigma \uparrow$ by 6%.
" " Si $\sigma \uparrow$ by 8%.

⇒ When compared to Ge Si is more sensitive to temperature but Si is widely used for high temperature applications and this is due to smaller value of leakage current in the Si.

END OF DAY

(32)

Doping

Trivalent (Acceptor) Impurities → B Al Ga In
Pentavalent (Donor) Impurities → P As Sb Bi

(B, P) ↓ more affinity toward Si.

⇒ It is the process of adding impurities to the pure semiconductor.

⇒ Doping increases carrier concn therefore increases the conductivity

$1:10^6$ or 1 in 10^6 or $\frac{1}{10^6}$

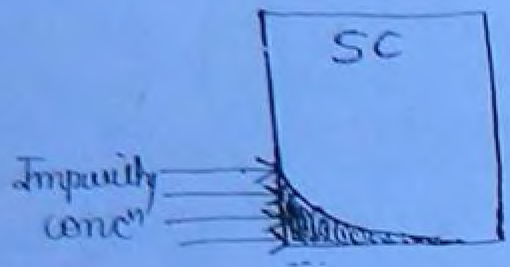
Standard Doping Concn :→

1. Moderate Doping ⇒ $1:(10^6 \text{ to } 10^8)$ → P N
2. Lightly Doped ⇒ $1:10^{11}$ → $\bar{P}$ $\bar{N}$
3. Heavily (Highly) Doped ⇒ $1:10^3$ → $\overset{+}{P}$ $\overset{+}{N}$

⇒ The minimum doping required to convert intrinsic semiconductor into extrinsic semiconductor is $1:10^8$.

* with $1:10^8$ Doping in Ge σ ↑ by 12 times
  with $1:10^7$ Doping in Ge σ ↑ by 120 times

Doping Profile :→



In Intrinsic semiconductor there will be always unequal distribution of charge carriers and therefore it has only the diffusion current.

⇒ The impurity is added to the semiconductor is called Doping profile.

⇒ The Doping profile can be Homogeneous or Non-homogeneous.

⇒ The Doping profile will be maximum on the surface where the profile is introduced and gradually decreases into the depth of the semiconductor

⇒ The doping profile must introduce the built in electric field (internal electric field). So the semiconductor will now exhibit the drift current.

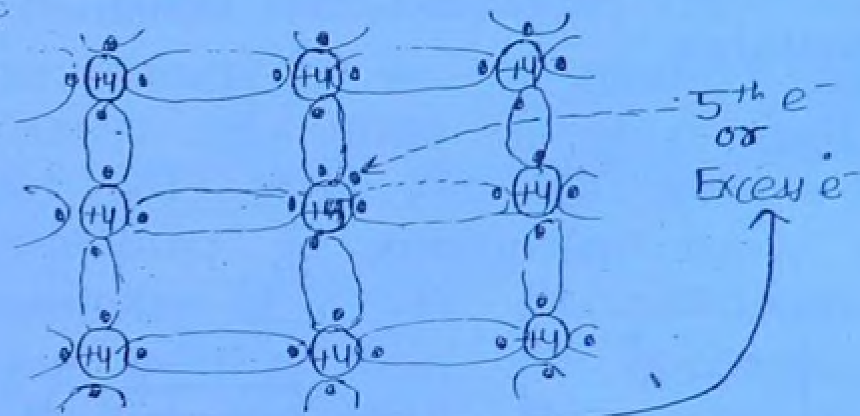
Extrinsic Semiconductor

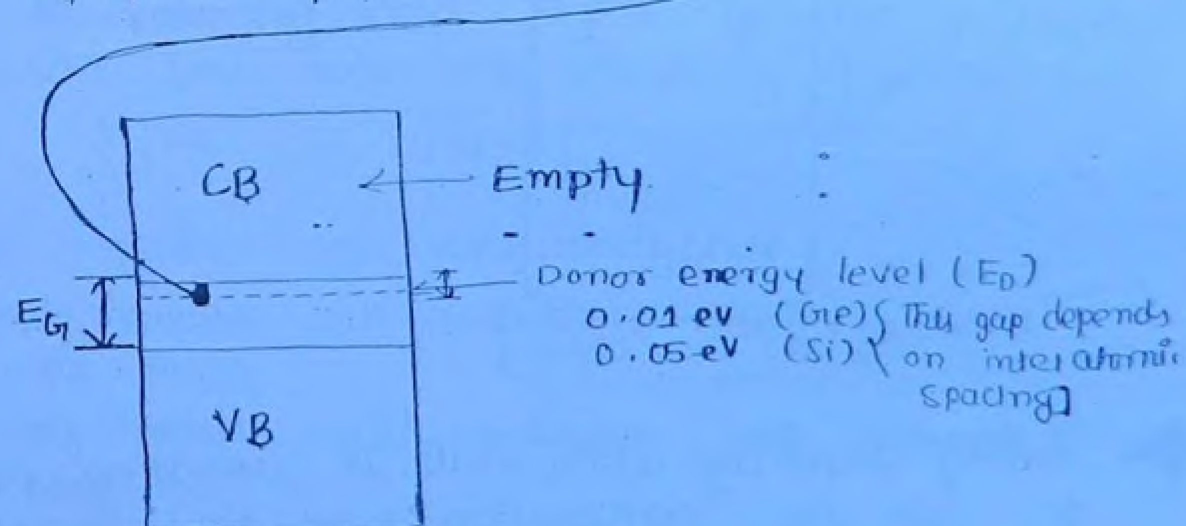
or Doped Semiconductor (or) Degenerated SC
or Impurity Semiconductor (or) Compensated SC.
or Artificial Semiconductor

N-type Semiconductor (or) DONOR

⟹ The Impurity is pentavalent (5^{th} group).

crystalline Structure at T=0K





⟹ Donor energy level is a discrete energy level created thus below the conduction band

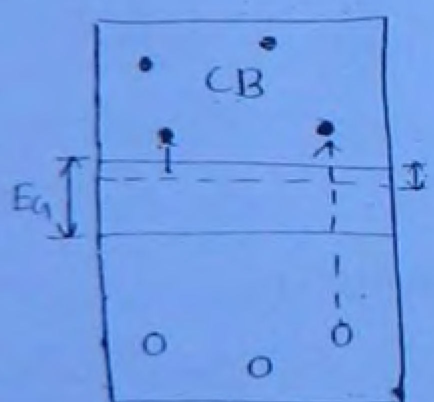
⟹ Donor energy level (E_D) denotes the energy level of all the pentavalent atoms added to the pure semiconductor.

⇒ At T=0K the fifth e⁻ of all the impurity atom will be existing in the donor energy level.

⇒ The additional energy required to detect the fifth e⁻ from its orbit is equal to 0.01 eV for Ge & 0.05 eV for Si.

⇒ At 0K entire semiconductor behaves as perfect insulator.

At T=300K



n >> p

⇒ at T = 300K

➜ Every impurity atom will be donating one e⁻ into the conduction band and therefore N-type is also called Donor.

➜ Donor level ionisation means the 5^{th} e⁻ moving from donor energy level into conduction band.

⇒ Donor level ionisation increases with temperature. (As temp. is increases from 0K to 300K more & more 5^{th} e⁻ will be moving from donor energy level into conduction band.)

→ Donor level ionisation is completed at 300K :
(i.e 5th e^- of all the impurity atom have shifted into the conduction band)

→ Above 300K, there is no donor level ionisation

⇒ As temperature is increasing from 0K to 300K the 5th e^- of the impurity atom will be moving from donor energy level into conduction band (due to donor level ionisation) and because of thermal energy a no. of covalent bonds will be broken and equal no. of e^- and holes are created and these e^- will move from valency band to conduction band so that the concentration of e^- in the conduction band is far greater than the concentration of holes in the valency band. Hence e^- are majority carriers and holes are minority carriers

{ For IES only }

⇒ ∴ N- Negative - type semiconductor

⇒ Majority carrier will contribute more current and less noise

⇒ Minority carrier will contribute less current & more noise

⇒ Minority carrier noise is thermal noise and it increases with the temperature.

⇒ In N-type SC current is predominating dominated by the flow of e^-

⇒ The condn for N- type SC is

$$n > n_i$$

$$p < n_i$$

⇒ In N-type semiconductor as e^- conc^n increasing above n_i, the hole conc^n. will be falling below n_i and this is due to a large no. of recombination

→ According to law of electrical Neutrality

$$\Rightarrow \boxed{N_D + P = N_A + n}$$

In N-type SC.

$$N_A = 0$$

$$\boxed{n = N_D + p}$$ {mainly used for IES}

$$\Rightarrow \boxed{\simeq n > N_D}$$

$$\Rightarrow \boxed{n \approx N_D}$$ { For other exams }

↑ Donor concentration.

↓ It denotes the no. of pentavalent atoms added to the pure semiconductor

$$\Rightarrow \boxed{N_D = \text{Total No. of atom/cm}^3 \times \text{Impurity ratio}}$$

⇒ The conductivity of N-type SC is ⇒

$$\sigma_n = nq\mu_n + pq\mu_p \quad \mho/cm$$

$$\Rightarrow \boxed{\sigma_n \approx N_D q \mu_n \quad \mho/cm}$$

⇒ In N-type semiconductor the free e^- concn is approximately equal to Donor concn ($n \approx N_D$)

⇒ Minority carrier conductivity is almost negligible.

Considering Si crystal.

when pure,

$$n = p = n_i = 1.5 \times 10^{10}/cm^3$$

⇒ By adding Donor impurity $1 : 10^6$

$$N_D = 5 \times 10^{22} \times \frac{1}{10^6} = 5 \times 10^{16} \text{ atom}/cm^3$$

⇒ Total Impurity atoms = 5×10^{16} atom/cm3

⇒ No. of 5^{th} e^- = 5×10^{16} atom/cm3

⇒ Due to Donor level ionisation e^- moving donor energy level into conduction band = 5×10^{16} atom/cm

⇒ Due to temp let 10^6 covalent Bond are broken

Then generated e^- ⇒ $10^6/cm^3$

" " holes ⇒ $10^6/cm^3$

e^-s moving from VB into CB = 10^6/cm

Total no. of e^- in CB = $5\times10^{16} + 10^6$

$= 5\times 10^{16}/cm^3$

Total no of holes in VB ⇒

$p = 10^6/cm^3$.

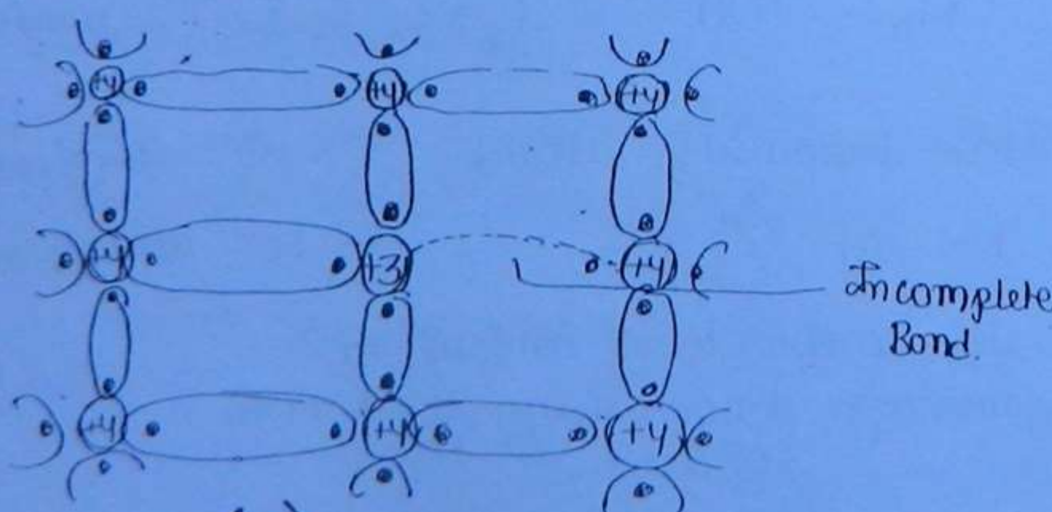
⇒ $n >> p$

P– type Semiconductor.

or

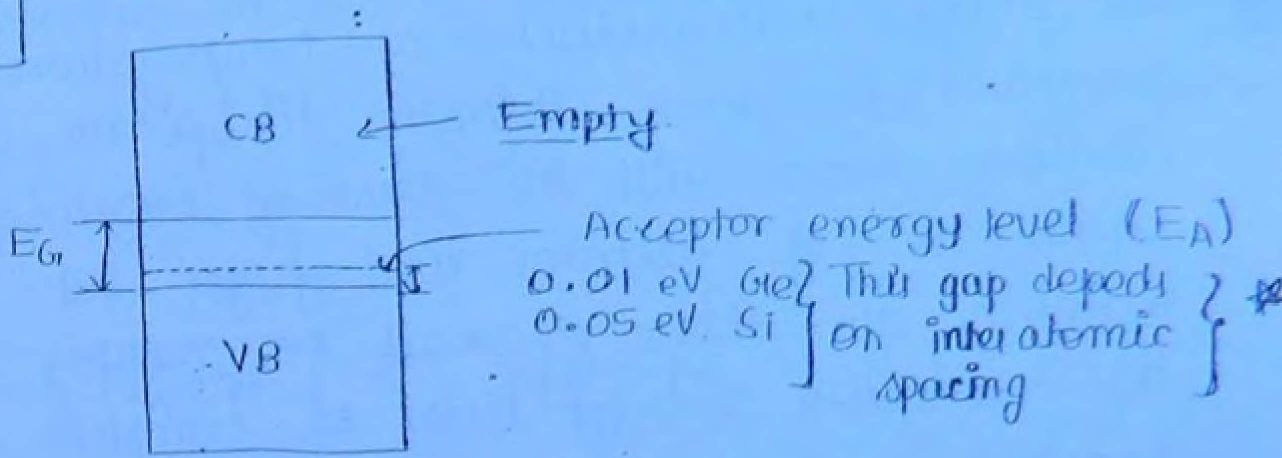
Acceptor – type SC.

⇒ Impurity is Trivalent.



at T = 0K

At T=0K

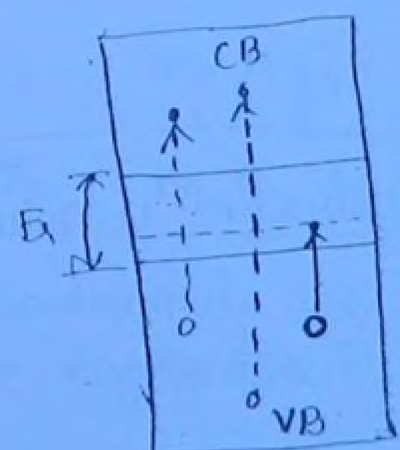


⇒ Acceptor energy level is created a discrete energy level created just above the valency band.

⇒ Acceptor energy level denotes the energy level of all the trivalent atoms added to the pure semiconductor

⇒ P- type semiconductor at (0 K) behaves as a insulator.

At T= 300K



⇒ $p >> n$

⇒ In p- type SC every impurity atom will be receiving one e⁻ to completes the covalent bonding & hence name acceptor

In p-type semiconductor as temperature is increased to 300K then a large no. of covalent bond will be broken creating equal no of electrons and holes but majority of these e^- will be moving into the acceptor energy level to complete its bonding and very few e^- will be moving from VB to CB. Hence hole concn in the VB is a far greater then e^- concn in the CB. Therefore holes are majority carriers and e^- are minority carriers.

{For conventional}

⇒ $p >> n$

⇒ positive – P – type SC

⇒ In p-type SC the current is mainly dominated by holes.

⇒ The condn for p-type is ⇒

$$\left\{ \begin{array}{l} p > n_i \\ n < n_i \end{array} \right\}$$

According to law of electrical Neutrality ⇒

$$N_D + P = N_A + n$$

In P- type

$$N_D = 0$$

⇒ $\boxed{P = N_A + n}$ ✱ $\boxed{P > N_A}$ (for IES)

$\boxed{P \simeq N_A}$ (For other exams)

↓ Acceptor concⁿ & it denotes the no. of trivalent atoms added to pure SC.

⇒ $\boxed{N_A = \text{Total No. of atom/cm}^3 \times \text{Impurity ratio}}$

The conductivity of p-type SC :→

$$\sigma_p = nq\mu_n + pq\mu_p \quad ℧/cm$$

✱ $\boxed{\sigma_p = N_A q \mu_p}$

⇒ The conductivity due to minority carriers is almost negligible.

Prob: A pure SC (Ge) is doped with donor impurities to extent of 1 : 10^7 calculate

(a) Donor concⁿ (N_D)

(b) e^- & hole concⁿ

(c) conductivity & resistivity of doped of SC.

(d) How many times the σ is increased due to doping.

Let total no of atoms = $4.421 \times 10^{22}/cm^3$

$n_i = 2.5 \times 10^{13}$ atoms/cm^3

$\mu_n = 3800\ cm^2/V\text{-sec}$

$\mu_p = 1800\ cm^2/V\text{-sec}$

Soln

N_D ⇒ Because of donor Impurity SC becomes n-type

(a) N_D = Total no of atoms/cm^3 × Impurity ratio

$$= \frac{4.421 \times 10^{22}}{10^7}$$

$N_D = 4.421 \times 10^{15}$ atoms/cm^3

(b) In N-type e^- concⁿ

$n \approx N_D$

$n = 4.421 \times 10^{15}$ atoms/cm^3

$np = n_i^2$

$$P = \frac{n_i^2}{n} = \frac{2.5 \times 10^{13}}{4.421 \times 10^{15}} = 1.41 \times 10^{11}/cm^3$$

(c) $\sigma_N = \mu_n N_D q = 3800 \times 4.421 \times 10^{15} \times 1.6 \times 10^{-19}$

$= 2.68\ \mho/cm$

$\rho = \frac{1}{2.68} = 0.373\ \Omega\text{-cm}$

(d)

(8) Before doping semiconductor is intrinsic

$$\sigma_i = n_i q (\mu_n + \mu_p)$$

$$\sigma_i = 2.5 \times 10^{13} \times 1.6 \times 10^{-19} [3800 + 1800]$$

$$\sigma_i = 0.0224\ \mho/cm$$

By adding doping concⁿ $1 : 10^7$ the conductivity increased $0.0224\ \mho/cm$ to $2.68\ \mho$.

$$\frac{2.68}{0.0224} \Longrightarrow \boxed{120 \text{ times}}$$ ✓

Prob A pure SC (Si) is doped with acceptor impurity to extent of 4 impurity atoms per every million of atom find its conductivity. (Ans 16)

Total no. of atoms $5 \times 10^{22} /cm^3$

$n_i = 1.5 \times 10^{10}$ atom/cm³

$\mu_n = 1300\ cm^2/V\text{-}sec$

$\mu_p = 500\ cm^2/V\text{-}sec$

Soln

$$N_A = 5 \times 10^{22} \times \frac{4}{10^6} = 2 \times 10^{13}\ atom/cm^3$$

$$\sigma_p = N_A q \mu_p$$

$$= 2 \times 10^{13} \times 1.6 \times 10^{-19} \times 500$$

$$\boxed{\sigma_p = 16\ \mho/cm}$$ Ans

Date 11.09.201

Prob In a semiconductor at room temp the intrinsic conc^n & intrinsic resistivity are $1.5 \times 10^{16}/m^3$ and $2 \times 10^3 \Omega$-m resp. it is converted into an extrinsic SC if a doping conc^n of $10^{20}/m^3$ for the extrinsic semiconductor.

(i) calculate minority carrier conc^n

(ii) electron mobility

(iii) Resistivity of doped SC.

(iv) minority carrier conc^n when its temp is increased to a value where there intrinsic conc^n is doubled. Assume the mobility of minority carriers is equal to the majority carrier mobility.

Sol^n (i) minority carrier conc^n $(p) = \dfrac{n_i^2}{n}$

$$p = \frac{(1.5 \times 10^{16})^2}{10^{20}}$$

$$p = \frac{2.25 \times 10^{32}}{10^{20}}$$

$$\boxed{p = 2.25 \times 10^{12}/m^3}$$

(ii)

$\mu_n = \mu_p = \mu$

$$\rho_i = \frac{1}{n_i q(\mu_n + \mu_p)} = \frac{1}{n_i q \, 2\mu}$$

$$\mu = \frac{1}{2 \times 10^3 \times 1.5 \times 10^{16} \times 2} = \boxed{0.1042}$$

(iii) $$\rho_{doped} = \frac{1}{\sigma_{doped}} = \frac{1}{\text{Doping conc}^n \times q \times \mu} = \frac{1}{10^{20} \times 1.6 \times 10^{-19} \times 0.1042}$$

$= 0.5996 \ \Omega$-m

(iv) Minority carrier conc^n $= \dfrac{(2n_i)^2}{10^{20}} = 9 \times 10^{12}/m^3$

Date: 11.09.2[illegible]

Prob In a semiconductor at room temp the intrinsic conc^n & intrinsic resistivity are $1.5 \times 10^{16}/m^3$ and 2×10^3 Ω-m resp. It is converted into an extrinsic SC if a doping conc^n of $10^{20}/m^3$ for the extrinsic semiconductor.

(i) calculate minority carrier conc^n
(ii) electron mobility
(iii) Resistivity of doped SC
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$$\boxed{p = 2.25 \times 10^{12}/m^3}$$

(ii)

$$\mu_n = \mu_p = \mu$$

$$\rho_i = \frac{1}{n_i q (\mu_n + \mu_p)} = \frac{1}{n_i q \, 2\mu}$$

$$\mu = \frac{1}{2 \times 10^3 \times 1.5 \times 10^{16} \times 2} = \boxed{0.1042}$$

(iii) $\rho_{doped} = \frac{1}{\sigma_{doped}} = \frac{1}{\text{Doping conc}^n \times q \times \mu} = \frac{1}{10^{20} \times 1.6 \times 10^{-19} \times 0.10[illegible]}$
$= 0.5996$ Ω-m

(iv) Minority carrier conc^n $= \frac{(2n_i)^2}{10^{20}} = 9 \times 10^{12}/m^3$

Ques A Si SC is doped with donor Impurities with resultant in doping profile as $\boxed{n = Gx}$: $n >> n_i$ the sample is placed isolated find built in E.F. as a function of x also calculate field at $x = 1\mu m$ at room temperature.

Sol

$n = Gx$

$n >> n_i$

SC is N-type

$J_n = J_{n(Diff)} + J_{n(Drift)}$

$J_n = nq\mu_n E + qD_n \frac{dn}{dx}$

Since Sample is isolated

$J_n = 0$

$n = Gx$

$\therefore \frac{dn}{dx} = G$

$0 = Gxq\mu_n + qD_n G$

$x\mu_n E = -D_n$

$E = \frac{-D_n}{\mu_n \cdot x}$

but $\frac{D_n}{\mu_n} = V_T$

$\boxed{E = -\frac{V_T}{x}}$

at $x = 1\mu m$

$E = -\frac{V_T}{1 \times 10^{-6}}$

$E = -10^6 V_T$ volt/m

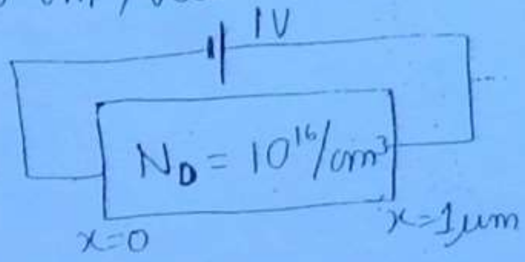
$E = -10^6 \times 10^{-3} \times 26 \Rightarrow -26 \times 10^3$

$\boxed{E = -2.6 \times 10^4 \text{ volt/m}}$

Prob The Si sample with unit cross sectional area given below is under thermal equilibrium the following information is given

$T = 300K$, $q = 1.6 \times 10^{-19}$, $V_T = 26\ mV$

$\mu_n = 1350\ cm^2/V sec$



(1) The magnitude of the E.F. at $x = 0.5\ \mu m$ is ____

(2) The magnitude of e drift current density at $x = 0.5\ \mu m$ ____

soln

[illegible]

$$\epsilon = \frac{0.5}{0.5 \times 10^{-6}} = 10\ kV/cm$$

$J_{n(Drift)}$ at $x = 0.5\ \mu m$

$$= nq\mu_n \epsilon$$

$$= 10^{16} \times 1.6 \times 10^{-19} \times 1350 \times 10 \times 10^3$$

$$J_{n(Drift)} = 2.16 \times 10^4\ A/cm^2$$

Minimum value of conductivity in a SC. {ITO}

$\Rightarrow \quad \sigma = nq\mu_n + pq\mu_p \longrightarrow (1)$

By mass action law.

$$p = \frac{n_i^2}{n} \quad \text{--- (2)}$$

substitute in eq (1) & (2)

$$\sigma = nq\mu_n + \frac{n_i^2}{n}\mu_p \cdot q \rightarrow (3)$$

Differentiating eq w.r.t 'n'

$$\frac{d\sigma}{dn} = q\mu_n + \left(-\frac{1}{n^2}\right) n_i^2 q\mu_p$$

$$\frac{d^2\sigma}{dn^2} = 0 + \left(\frac{2}{n^3}\right) n_i^2 q\mu_p$$

Since II^{nd} derivative is +ve, we get $cond^n$ for minimum conductivity

=) The minimum conductivity can be obtain by

$$\frac{d\sigma}{dn} = 0$$

$$0 = q\mu_n + \left(-\frac{1}{n^2}\right) n_i^2 q\mu_p$$

$$\mu_n = \frac{n_i^2}{n^2}\mu_p \Rightarrow n^2 = n_i^2 \frac{\mu_p}{\mu_n}$$

$$\Rightarrow \boxed{n \text{ or } n_0 = n_i\sqrt{\frac{\mu_p}{\mu_n}}} \longrightarrow (A)$$

⇒ Eqⁿ Ⓐ denotes the concⁿ of e^- in the SC and conductivity is minimum

⇒ eqⁿ Ⓐ also denotes thermal equilibrium e^- if the sc is p-type

⇒ Substituting eq Ⓐ in eq ②

$$p = \frac{n_i^2}{n}$$

$$p = \frac{n_i^2}{n_i\sqrt{\frac{\mu_p}{\mu_n}}}$$

$$\Rightarrow \boxed{p = n_i\sqrt{\frac{\mu_n}{\mu_p}}} \longrightarrow (B)$$

⇒ eq Ⓑ denotes the concⁿ of holes in SC when conductivity is minimum

⇒ eq Ⓑ also denotes thermal equilibrium holes if semiconductor is N-type.

⇒ Substituting Ⓐ & Ⓑ in eq ① we get eqⁿ for minimum conductivity.

$$\sigma_{min} = n_i\sqrt{\frac{\mu_p}{\mu_n}}\, q\mu_n + n_i\sqrt{\frac{\mu_n}{\mu_p}} \cdot q\mu_p$$

$$\sigma_{min} = n_i q\left[\sqrt{\mu_n\mu_p} + \sqrt{\mu_n\mu_p}\right]$$

$$\Rightarrow \boxed{\sigma_{min} = 2 q n_i \sqrt{\mu_n\mu_p}}$$

Prob A semiconductor has following parameter

$\mu_n = 7500\ cm^2/v\text{-}sec$

$\mu_p = 300\ cm^2/v\text{-}sec$

$n_i = 3.6 \times 10^{12} / cm^3$

find ① min σ

② hole concⁿ in SC when σ_{min}.

③ Thermal equilibrium e^{-1}

soln

$$\sigma_{min} = 2 q n_i \sqrt{\mu_n \mu_p}$$

$$= 2 \times 1.6 \times 10^{-19} \times 3.6 \times 10^{12} \sqrt{7500 \times 300}$$

$$= 2 \times 1.6 \times 3.6 \times 10^{-5} \sqrt{75 \times 3}$$

$$= 3.2 \times 3.6 \times 10^{-5} \times \sqrt{225}$$

$$= 3.2 \times 3.6 \times 15 \times 10^{-5} = 48 \times 3.6 \times 10^{-5}$$

$$= 172.8 \times 10^{-5} = 1.72 \times 10^{-3}\ \mho/cm$$

~~= 172~~

$$P = n_i \sqrt{\frac{\mu_n}{\mu_p}} = 3.6 \times 10^{12} \sqrt{\frac{7500}{300}} = 3.6 \times 5 \times 10^{12}$$

$$P = 18 \times 10^{12} = 1.8 \times 10^{13}$$

$$n = n_i \sqrt{\frac{\mu_p}{\mu_n}} = \frac{3.6 \times 10^{12}}{5} = 7.2 \times 10^{11}$$

GERMANIUM – Si Crystal. {Not for GATE & IES}

⇒ When Ge is added to Si or Si is added to Ge we get Ge-Si crystal the type of bonding provided is covalent bonding.

⇒ At 0 K they behave as insulator

⇒ At room temperature they behave as intrinsic semiconductor.

⇒ **When SC is subjected to Donor or acceptor impurities**

⇒ In Intrinsic SC :–

(i) if $N_A = N_D$ is applied.

⇒ SC remains intrinsic.

(ii) if $N_A > N_D$ is applied

⇒ SC turns P-type

(iii) if N_A N_D is applied

⇒ SC turns N-type

Ques → A P-type SC having $N_A = 2 \times 10^{16}/cm^3$ is subjected to donor impurity or concⁿ of $N_D = 2.5 \times 10^{16}/cm^3$ then SC is N-type & e^- concⁿ is $0.5 \times 10^{16}/cm^3$

Quesⁿ A 85 gm of P-type Ge crystal exhibit a resistivity of 5 Ω-cm at room temp. by uniform Sb doping it is converted into N-type SC having 1 Ω-cm resistivity at 300K. if each atom of the initial acceptor impurity is exactly neutralized by 1 atom of Sb. find in μg, the amt of antimony required {25 yrs ago In IE}

The density of Ge 5.32 gm/cm³ / No. of Sb atom/gm = 5×10^{21}

$\mu_n = 3800$, $\mu_p = 1800$, $n_i = 2.5 \times 10^{13}/cm^3$, $q = 1.6 \times 10^{-19} C$

soln Before doping the SC is P-type with resistivity of 5Ω-cm & therefore it N_A or density or hole concn

$$N_A = \frac{1}{\rho_p \cdot q \mu_p}$$

$$N_A = \frac{1}{5 \times 1.6 \times 10^{-19} \times 1800}$$

P ⇒ $N_A = 6.944 \times 10^{14} / cm^3$

By adding Sb doping the P-type SC is converted into N-type SC with ρ of 1Ω-cm & N_D or e^- concn

$$N_D = \frac{1}{\rho_n q \mu_n}$$

$$n = N_D = \frac{1}{1 \times 1.6 \times 10^{-19} \times 3800} = 16.45 \times 10^{14} / cm^3$$

Total no of Sb atom reqd = $N_A + N_D$

$= (6.944 + 16.45) \times 10^{14}$

$= 23.39 \times 10^{14} / cm^3$

⇒ Net No. of e^- in SC observed neutralising the initial holes of P-type SC

⇒ The No. of Sb reqd is above.

$$\text{Volume} = \frac{wt}{density}$$

25 gm crystal of Ge has a

$Vol = 25/5.32 = 4.699 \ cm^3$

Total no of Sb reqd

↳ wt $23.39 \times 10^{14} \times 4.699$ atom/cm³ = 109.928×10^{14} atoms

⇒ $109.928 \times 10^{14} / 6 \times 10^{21}$ → 2.1985 μgm

Carrier concⁿ : in intrinsic semiconductor :⇒

⇒ Carrier concⁿ means the charge carrier responsible for the conductivity

⇒ In intrinsic SC carrier concⁿ means e^- concⁿ and hole concⁿ.

Effect of temperature on carrier concⁿ in intrinsic sc

In intrinsic SC

$$n = p = n_i$$

but $n_i \propto T^{3/2}$

$\therefore$ $n_i \uparrow$ with $T \uparrow$

& $p \uparrow$ with $T \uparrow$

⇒ In intrinsic SC carrier concⁿ increases with temp

Effect of temperature on conductivity of intrinsic sc.

In intrinsic SC

$$\sigma_i = n_i q [\mu_n + \mu_p]$$

$$\sigma_i \propto n_i$$

but $n_i \propto T^{3/2}$

$\therefore$ $\sigma_i \uparrow$ with $T \uparrow$

⇒ In intrinsic SC conductivity increases with temp.

Carrier concⁿ in extrinsic SC

In extrinsic SC carrier concⁿ means majority carrier concⁿ.

Effect of ~~temp.~~ doping in extrinsic SC

N-type SC :→

$\sigma_N = N_D q \mu_n$

$\Rightarrow \boxed{\sigma_n \propto N_D}$

P-type SC :→

$\sigma_P = N_A q \mu_p$

$\boxed{\sigma_P \propto N_A}$

⟹ Conductivity increases with doping in extrinsic SC.

$1:10^8$	$\sigma \times 12$
$1:10^7$	$\sigma \times 120$
$1:10^6$	$\sigma \times 1200$
$1:10^5$	$\sigma \times 12K$
$1:10^4$	$\sigma \times 120K$
$1:10^3$	$\sigma \times 1200K$

→ A highly doped SC exhibits metallic properties i.e.

(1) larger conductivity
(2) Bipolar nature can be converted into unipolar.
(3) NTC converted into PTC of resistance.

~~Fact~~ ⟹ A highly doped SC behaves as a conductor.

Effect of Doping on majority & minority carrier

N type

majority carriers are $e^- \rightarrow n$

$n \approx N_D$

minority carriers are holes $\rightarrow p$

$$p = \frac{n_i^2}{n} = \frac{n_i^2}{N_D}$$

P-type

Majority carriers are holes → p

$p \approx N_A$

minority carrier are e^-s → n

$$n = \frac{n_i^2}{p} = \frac{n_i^2}{N_A}$$

⇒ Doping increases majority carrier concn and reduces the minority carrier concn.

Effect of temp. on majority & minority carriers

considering Si bar

when pure

$n = p = n_i = 1.5 \times 10^{10}/cm^3$

By adding Donor concn 1 : 10^6

$N_D = 5 \times 10^{22} \times \frac{1}{10^6}$

$N_D = 5 \times 10^{16}/cm^3$

SC turns N-type

In N-type SC at 300K

$n \approx N_D = 5 \times 10^{16}/cm^3$

$p = n_i^2/N_D = (1.5 \times 10^{10})^2/5 \times 10^{16} = 4500/cm^3$

Let temp. ↑ & 10^6 covalent bonds are broken

Thermally generated e^- ⇒ $10^6/cm^3$

" " holes ⇒ $10^6/cm^3$

Total no. of e^- in CB ⇒ $5 \times 10^{16}/cm^3 + 10^6/cm^3 \Rightarrow 5 \times 10^{16}/cm^3$

→ Increase in e^- concn (majority) is negligible

Total no of holes in VB $p = 4500/cm^3 + 10^6 = 10^6/cm^3$

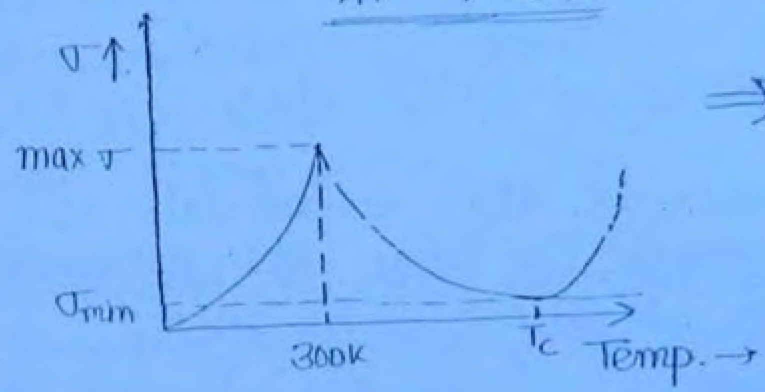
→ Increase in minority concn (hole) is very high.

⇒ In a SC majority carrier concⁿ is almost independent of temperature.

⇒ In a SC minority carrier concⁿ is still increases with temperature.

⇒ Effect of temp. on the conductivity of extrinsic semiconductor.

At T = 0K



⇒ characteristic curve

⇒ σ Vs Temp

T_C = Curie Temp.

At T = 0K Carrier concⁿ are zero and therefore σ is zero. an extrinsic SC at 0K is a ∴ insulator

At 0K < T < 300K.

As temperature is increasing because of thermal energy a no of covalent-bond will be broken and also majority and minority carriers are created and therefore the conductivity will be increases with temperature

At T = 300K

The conductivity of extrinsic semiconductor will become maximum.

when 300K < T < T_c.

- As temp. is increases mobility of charge carriers decreases and therefore conductivity decreases
- As temp is increasing, minority carrier concⁿ will increasing with temp.
- As temp is increasing majority carrier concⁿ will remain almost a const.

$T = T_c$: At $T = T_c$ | At $T = T_c$:

→ Minority carrier concⁿ approaches majority carrier concⁿ and extrinsic semiconductor will become intrinsic semiconductor but their conductivity slightly greater then σ_i.

→ At curie temperature the extrinsic SC will become intrinsic SC and the purpose of doping in the semiconductor lost.

→ **At $T > T_c$** .

→ Above curie temperature extrinsic SC is intrinsic & therefore the conductivity will be increasing with the temp.

* At very high temp. extrinsic SC will become intrinsic semiconductor.

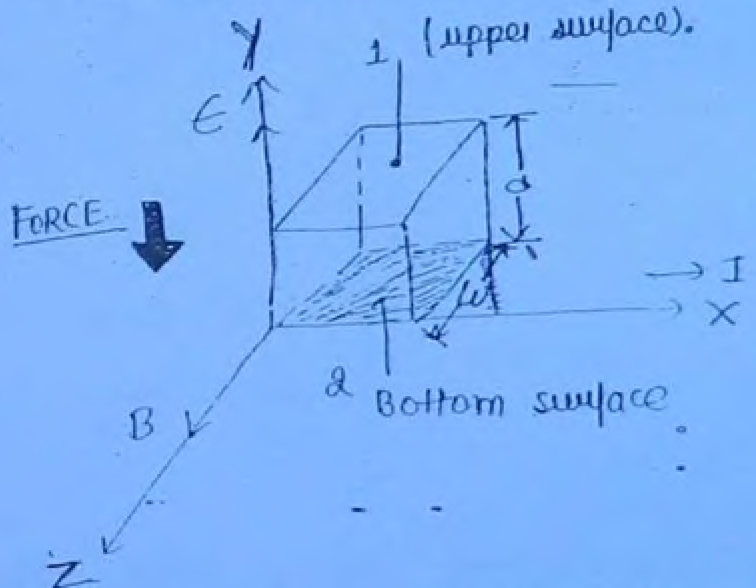
* At low temp. extrinsic SC as temp. is increasing the conductivity increases with temp.

* In extrinsic SC the conductivity decreases with temp. (Becoz temp. as temp is increasing mobility of charge carrier decreases).

HALL Effect

⇒ Hall effect states that — " If a specimen (metal or SC) carrying the current 'I' is placed in transverse magnetic field B. Then an electric field intensity 'E' is induced in a direction perpendicular to both I and B."

⇒ A current carrying metallic strip is placed in transverse magnetic field then an electric field intensity is induced in a direction ⊥ to both I & B



⇒ The specimen should be square or rectangular in shape

→ 'w' is width of the specimen

⇒ 'd' is height or thickness of the specimen and it is also the spacing between the bottom and upper surface

⇒ The current direction is taken on x- direction and magnetic field in z- direction and field intensity in y- direction

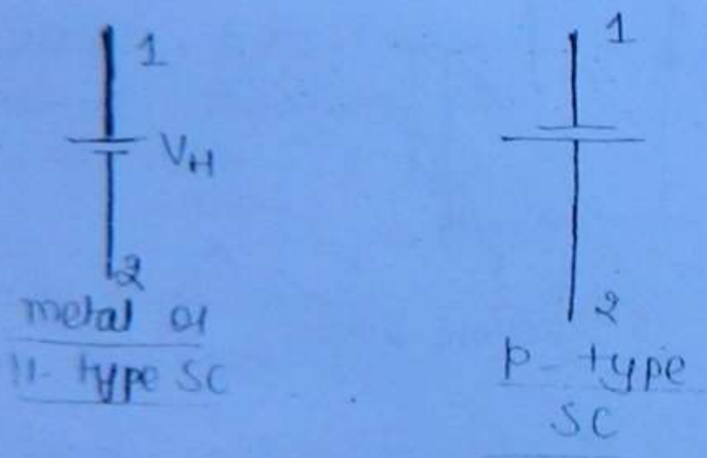
→ Direction of force is downward for e⁻ & holes because hole is valency e⁻ for taken with +ve charge

⇒ By using the hall experiment, we can determine

(1) whether the given specimen is a metal or SC.
(2) Concⁿ of charge carriers
(3) mobility of charge carriers.
(4) Magnetic flux density
(5) In designing of hall effect transducer
(6) To measure the signal power in EM wave

⇒ The polarity and magnitude of the induced hall voltage will indicate whether the given specimen ~~is metal or~~ SC.

⇒



⇒ Electric field intensity

$$|E| = \frac{|V_H|}{d} \text{ V/m}$$

⇒ Hall voltage V_H

⇒ $$V_H = Ed \text{ volts}$$

⇒ ⇒ $$V_H = \frac{BI}{\rho W} \text{ volts}$$

ρ → charged density.

$$\frac{1}{\rho} = R_H$$ Hall coefficient

$$\Rightarrow \boxed{V_H = \frac{I B R_H}{w}}$$

$$\Rightarrow \boxed{V_H \propto R_H}$$

⇒ From the Hall experiment mobility of charge carrier

$$\boxed{\mu = \frac{8}{3\pi} \sigma R_H}$$

$$\boxed{\mu \approx \sigma R_H}$$ { $\sigma \rightarrow$ conductivity of specimen }

⇒ <u>Applications</u> :→

→ Hall effect multiplier

→ Magnet-o-field meter.

⇒ <u>IES ONLY</u>

⇒ Magneto-field meter is an instrument used for measurement of magnetic flux density.

⇒ By using hall experiment we can measure magnetic flux density → $\boxed{H \propto B}$

⇒ By using hall experiment we can measure magnetic field intensity.

⇒ if the polarity of induced hall voltage is +ve for the bottom surface, the given specimen is <u>p-type sc</u>

⇒ Hall voltage is measured with respect to "bottom" surface of specimen.

⇒ For metal Hall voltage is -ve

⇒ For N-type SC Hall voltage is -ve

⇒ For P-type SC Hall voltage is +ve

⇒ For intrinsic semiconductor hall voltage is "zero". (PSU)

⇒ In Hall experiment if one input signal is applied in the form of current and another input signal is applied in the form of magnetic field then induced Hall voltage is equal to the product of two input signal and Hence Hall experiment can be used in designing of Hall-effect multiplier.

⇒ The charge density

$$\Rightarrow \boxed{\rho = \text{charge} \times \text{carrier conc}^n} \; C/m^3$$

⇒ Hall coefficient R_H

$$\boxed{R_H = \frac{1}{\rho} = \frac{1}{\text{charge} \times \text{carrier conc}^n}} \; m^3/C.$$

⇒ From the Hall experiment

$$\Rightarrow \mu \approx \sigma R_H$$

$$\Rightarrow \boxed{R_H \approx \frac{\mu}{\sigma}}$$

$$\boxed{\begin{array}{l} V_H \propto R_H \\ R_H \propto V_H \propto \frac{1}{\sigma} \end{array}}$$

(For metals)

→ σ is large, V_H is small (μV)

(For SC)

→ σ is small, V_H is large (mV).

⇒ Hall voltage is small [metals]

⇒ Hall voltage is large in [SC.]

⇒ The mobility of charge carrier can be experimentally found by using Hall effect

⇒ The mobility of charge carrier can be experimentally found by using Hayness - Schockley experiment

⇒ By using Hayness - Schokley experiment we can measure

→ Mobility of charge carrier

→ Diffusion const of charge carrier ($D = \mu V_T$, $D \propto \mu$)

(ITO):

Prob A doped SC specimen has Hall coefficient 3.6×10^{-4} m and resistivity 9×10^{-3} Ω-m assuming single carrier conduction, the mobility & density of charge carriers in the specimen approximately are given by ____

Soln

$R_H = 3.6 \times 10^{-4}$, $\rho = 9 \times 10^{-8}$

$$\mu = \sigma R_H = \frac{1}{9 \times 10^{-3}} \times 3.6 \times 10^{-4} = 0.4 \times 10^{-1}$$

$\mu =$ 0.04 $m^2/v\text{-}sec$

$$R_H = \frac{1}{q \cdot \text{carrier conc}^n}$$

$$\text{carrier conc}^n = \frac{1}{q R_H} = 1.73611 \times 10^{22}/m^3$$

Assuming single carrier conc^n

σ = carrier conc^n × q × μ

carrier conc^n = $\frac{\sigma}{q\mu}$

$= \frac{1}{\rho \times q \times \mu} = \frac{1}{9 \times 10^{-3} \times 1.6 \times 10^{-19} \times 0.04}$

carrier conc^n = $1.73611 \times 10^{22}/m^3$

(For IES)

Prob: Find the magnetic field in a rectangular SC specimen 4mm wide and 2mm thick & having hall coefficient of $10^{-3}\ m^3/C$ when a current 1mA is passed through the sample, a hall voltage of 2mV is obtained.

Soln:

$V_H = \frac{BI}{\rho w}$

$V_H = \frac{R_H B}{w}$

$2 \times 10^{-3} = \frac{10^{-3} \times B \times 10^{-3}}{4 \times 10^{-3}}$

$B = \frac{8 \times 10^{-3}}{10^{-3}} = 8\ Wb/m^2$

Prob Find the magnetic : of the hall coefficient in a N-type Ge bar of width 3mm and height 2mm assume $B = 0.9\ wb/m^2$, $\epsilon = 5V/cm$ and current $I = 1.5mA$.

Soln

$$V_H = \frac{BR_H}{\omega}$$

$$V_H = \epsilon d = 5\times10^{+2} \times 2\times10^{-3}$$

$$V_H = 10^3\times10^{-3} = 1V.$$

$$1 = \frac{0.9 \times R_H \times I}{3\times10^{-3}}$$

$$R_H = \frac{3\times10^{-3}}{0.9} = .99\times10^{-2} = 9.9\times10^{-1}$$

$\times 1.5\times10^{-3}$

$$R_H = 2.22\ m^3/c$$

(ii) page

Soln (5) $\omega = 2mm$, $d = 0.2mm$

$I = 10mA$ $B = 0.1\ wb/m^2$

$V_H = -1.0mV$, $R_H = ?$, $n = ?$

Soln

$$V_H = \frac{BIR_H}{\omega}$$

$$R_H = \frac{|V_H|\omega}{B \cdot I} = \frac{+1.0\times10^{-3}\times2\times10^{-3}}{0.1\times10\times10^{-3}}$$

$$R_H = 2\times10^{-3}$$

$$n = \frac{1}{qR_H} = \frac{1}{1.6\times10^{-19}\times2\times10^{-3}}$$

$$n = 312.5\times10^{19}/m^3$$

Classification of Semiconductor.

Direct Band gap SC (DBG – SC)

1) During the recombination energy is dissipated in the form of light e.g. GaAs.

2) other examples GaN, GaSb, InAs, ZnS, CdS, CdSe, (InP)

3) During recombination most of the falling e^- will be directly falling from CB to VB and release the energy in the form of light and very few e^- will be colliding with crystal of atom & these crystal will absorbing energy in the absorbing energy from falling e^- and gets heated up & they will release the energy in the form of heat (99% light & 1% heat)

4) During the recombination most of the falling e^- will be directly releasing the energy in the form of light & therefore called direct Band gap SC

The energy of falling e^- changes (both K.E & P.E. changes)

Indirect band gap SC (IBG – SC)

① During the Recombination energy is dissipated in the form of heat. (Ge, Si)

② other excamples AlP, PbS, AlAs, AlSb, (GaP) PbSe.

③ During recombination most of falling e^- will be colliding with crystal of the atom and these crystal will be absorbing the energy from falling e^- And they dissipate the energy in the form of heat But very few falling e^- will be escaping the collision and they will directly fall into the valency band & energy is released in the form of light (99% heat & 1% light)

④ The falling e^- are indirectly responsible in releasing the energy to the crystal of atom in the form of heat & therefore called indirect band gap – SC

same as

(6) The direcⁿ of falling e⁻ will remain the same but also the part of e⁻ will remain the same.	(6) The direcⁿ of falling e will remain the same but also the part of e⁻ slightly changes because of collision.

(7) The momentum of the falling e⁻ changes for both SC.

(8) Relatively carrier lifetime is less	(8) Relatively carrier lifetime is large.

⇒ * Si is never used in fabrication of LED & LASER because it is Indirect band gap SC.

* Si is not used for fabrication of following devices

→ LED

→ Tunnel diodes

→ Varactor diode

→ PIN Diode

→ Gunn Diode

→ IMPATT Diode

→ LASER

* GaAs is a e.g. for DBG-SC

(1) DBG-SC ✓

(2) IBG-SC

(3) Wide-band gap-SC.

(4) Narrow band gap-SC

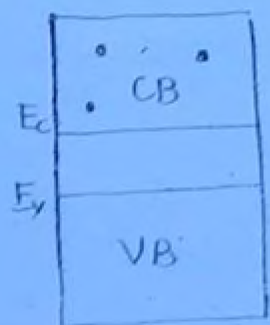
*

Prob

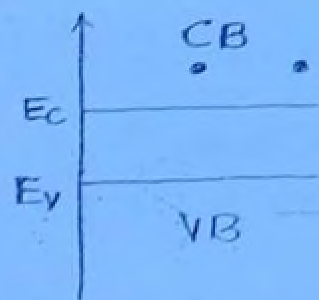
Semiconductor LASER are fabricated with :→

(a) → DBG-SC with larger time constt. → Ans
(b) → DBG-SC with smaller time constt
(c) → IBG-SC with smaller time constt.
(d) → IBG-SC with larger time constt

Equation for concⁿ of e⁻ in the CB.



Approx Energy Band Diagram



Exact Energy Band Diagram

→ E_c minimum energy of the conduction band
→ E_v maximum energy of the valency band
→ Energy possess by free e^- in the conduction band has energy in the range of E_c to $+\infty$.
→ The eqⁿ for concⁿ of e^- in the conduction band

$$\Rightarrow \boxed{n = N_c e^{-(E_c - E_f)/KT}}$$

E_F → Fermi energy in eV.

N_c → material constt. it is function of temp.

$$N_c = 2\left(\frac{2\pi K T m_n}{h^2}\right)^{3/2}$$

$$N_c = 2\left(\frac{2\pi K m_n}{h^2}\right)^{3/2} T^{3/2}$$

m_n → effective mass of e^-

is the mass of e^- when e^- is revolving in the given material. (effective mass)

For Si

$$\left(\frac{m_n}{m}\right) = 1.08$$

→ Effective mass of e^- is always greater then rest mass of e^-.

$m \rightarrow 9.1 \times 10^{-31}$ kg → rest mass of e^-

$$m_n = 1.08m$$
$$= 1.08 \times (9.1 \times 10^{-31}) \text{ kg}$$

$$\Rightarrow \boxed{m_n = 1.08 \times 9.1 \times 10^{-31}}$$

→ N_c is approx equal to the density of states in the CB.

Equation for concⁿ of holes in VB. :⇒

→ The energy possessed by holes in VB is $-\infty$ to $+E_v$

→ The eqⁿ for concⁿ of holes in VB is given by.

$$\boxed{P = N_v e^{-[E_F - E_v]/KT}}$$

→ N_v is a material constt. and it is a funcⁿ of temp.

$$N_v = 2\left(\frac{2\pi KT m_p}{h^2}\right)^{3/2} = 2\left(\frac{2\pi K m_p}{h^2}\right)^{3/2} T^{3/2}$$

$m_p \rightarrow$ effective mass of the hole.

For Si

$$\left(\frac{m_p}{m}\right) = 0.56$$

$$m_p = 0.56\, m$$

$m \rightarrow$ is the mass of hole

$m \rightarrow 1.6 \times 10^{-27}$ kg.

$$\boxed{m_p = 0.56 \times 1.6 \times 10^{-27}}$$

→ N_v is approximately equal to density of states in the valency band

NOTE :→ mass of the hole is equal to mass of proton

→ Effective mass of hole is always greater then effective mass of e^- $\Rightarrow \boxed{m_p > m_n}$

Derive an equation for intrinsic conc^n (n_i). :→

$$n = N_c\, e^{-[E_c - E_F]/KT} \rightarrow ①$$

$$p = N_v\, e^{-[E_F - E_v]/KT} \rightarrow ②$$

Multiplying eq ① & ②

$$np = N_c N_v\, e^{-E_c + E_v/KT}$$

$$np = N_c N_v\, e^{-\left[\frac{E_c - E_v}{KT}\right]} \left[\Rightarrow \text{but } E_c - E_v = E_g\right]$$

& $np = n_i^2$

$$\Rightarrow n_i^2 = N_c N_v\, e^{E_g/KT} \Rightarrow \boxed{n_i^2 = N_c N_v\, e^{-E_g/KT}}$$

but $N_c N_v = 2\left(\frac{2\pi \bar{K} T m_n}{h^2}\right)^{3/2} \cdot 2\left(\frac{2\pi \bar{K} T m_p}{h^2}\right)^{3/2} T^3$

$\Rightarrow A_0 T^3$

$\Rightarrow$ $\therefore n_i^2 = A_0 T^3 e^{-E_G/KT}$

where $\therefore \Rightarrow$ $A_0 = 4\left(\frac{2\pi \bar{K}}{h^2}\right)^3 (m_n m_p)^{3/2}$

FERMI ENERGY :-> (E_F)

→ Fermi energy is defined as the maximum energy possessed by the e^- at 0K

(Or)

→ Fermi energy is also defined as the maximum kinetic energy by the e^- at 0K.

E_F = max K.E.

$= \frac{1}{2} m v_{max}^2$

Max velocity of e^- or velocity of e^- } $v = \sqrt{\frac{2E_F}{m}}$ m/s.

↑ eq^n for velocity of e^- in terms of fermi energy.

(OK)

⇒ Fermi energy is also define as the energy possessed by the fastest moving e^- at 0K.

Fermi Dirac function [$f(E)$] :→

→ It is also called fermi dirac probability function.

⇒ The fermi dirac function for a metal or SC is given by

$$\Rightarrow \boxed{f(E) = \frac{1}{1 + e^{(E - E_F)/KT}}}$$

E → Energy possessed by e^- in eV.

→ Fermi dirac func^n is used to find the probability of e^- existing as a function of energy level.

→ At T=0K, we get two conditions.

(i) if $E > E_F$

$$f(E) = \frac{1}{1+e^{+\infty}} = \frac{1}{1+\infty} = 0 \text{ (or) } 0\%$$

⇒ This indicates at T=0K, no e^- are available in the material with energies greater then E_F.

(ii) if $E < E_F$

$$f(E) = \frac{1}{1+e^{-\infty}} = \frac{1}{1+0} = 1 \text{ (or) } 100\%$$

⇒ This indicates at T=0K, e^- are available with energies less then E_F.

At $T \neq 0K$ (or) **$T > 0K$**

If $E = E_f$:→

$$f(E) = \frac{1}{1+e^0} = \frac{1}{1+1} = \frac{1}{2} \text{ or } 0.5 \text{ or } 50\%$$

⇒ The above analysis indicates when $T > 0K$ e^- may or may not be available with energies $E = E_f$.

⇒ Fermi level is the energy level with 50% probability of being field if no forbidden band exist.

⇒ In metal $f(E) = 1$ or 100%

⇒ In SC, the probability of e^- exiting is $f(E)$ then probability of hole exiting is $1 - f(E)$.

Fermi level in Intrinsic Semiconductor. :→

$$n = p$$

$$N_c e^{-[E_c - E_F]/KT} = N_V e^{-[E_F - E_V]/KT}$$

$$\frac{N_c}{N_V} = e^{-2E_F + E_V + E_c / KT}$$

$$\ln\left(\frac{N_c}{N_V}\right) = \frac{E_c + E_V - 2E_f}{KT}$$

$$E_F = \frac{E_c + E_V}{2} - \frac{KT}{2} \log \frac{N_c}{N_V}$$

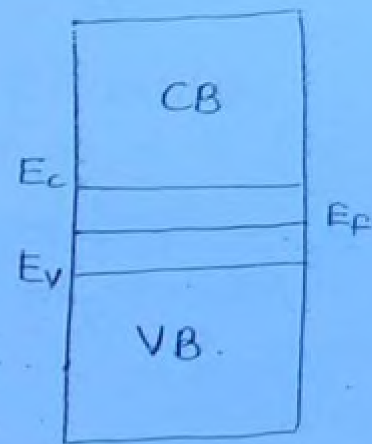
⇒ In intrinsic SC fermi level depends only on temperature.

Case - I

let $\left\{ \begin{array}{l} m_n = m_p \\ N_c = N_v \end{array} \right\}$ ⇒

∴ $\frac{KT}{2} \log \frac{N_c}{N_v} = 0$

⇒ ✱ $E_f = \frac{E_c + E_v}{2}$

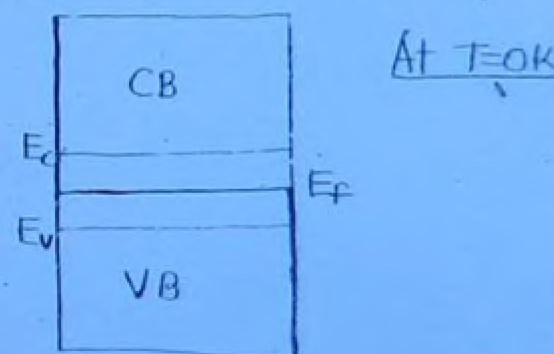


⇒ The fermi level will now existing at the centre of energy gap

Case - II :→

let T = 0K

⇒ ✱ $E_f = \frac{E_c + E_v}{2}$



⇒ At T=0K, an intrinsic SC fermi level is existing at the centre of the energy gap.

⇒ At T=0K, carrier concⁿ are zero and therefore conductivity is zero and intrinsic SC will behave as insulator.

NOTE → In intrinsic SC fermi level will be existing exactly at the centre of energy gap under 3 condⁿˢ

(1) $m_n = m_p$
(2) $N_c = N_v$
(3) T = 0K

✱✱

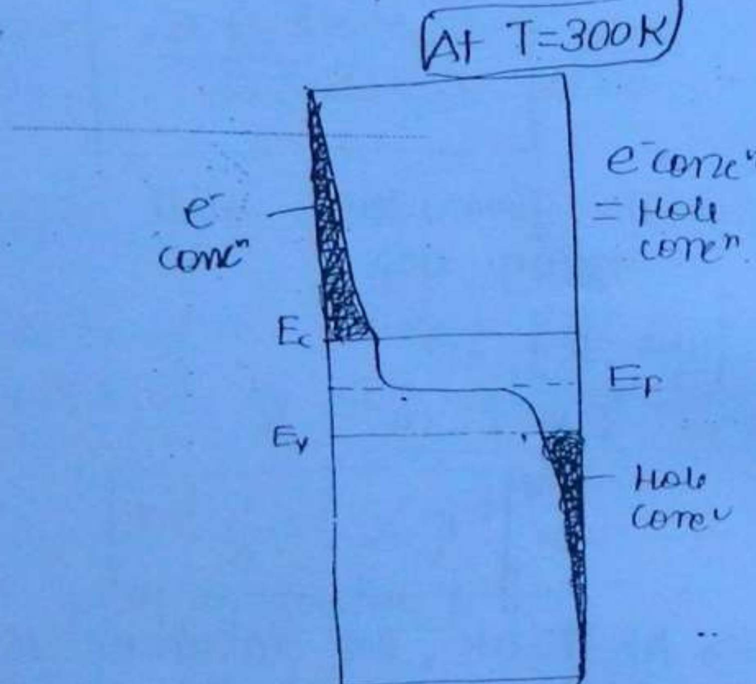
Case III

At T = 300K

$$E_F = \frac{E_c + E_v}{2} - \frac{KT}{2} \log_e \frac{N_c}{N_v}$$

where T = 300K

$$E_F = \frac{E_c + E_v}{2} - 150T \log_e \frac{N_c}{N_v}$$

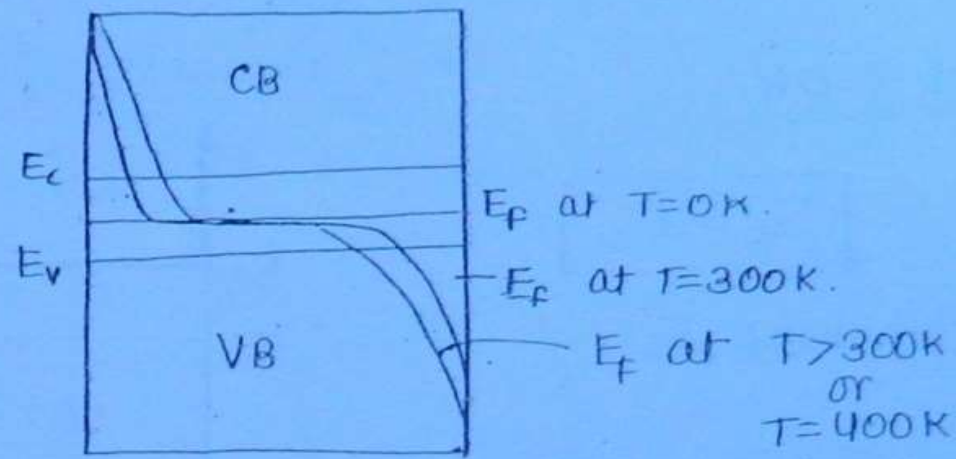


⇒ In intrinsic semiconductor at room temp, fermi level will be passing through the centre of energy gap

⇒ At room temp because of thermal energy, a no of covalent bond will be broken and equal no. of e⁻ and holes are created and there will be a conductivity in the SC.

Case IV.

(Fermi level positions at different temp.) :->



Fermi level in N-type SC. $\Rightarrow$

$$n \simeq N_D$$

$$N_c\, e^{-[E_c - E_F]/KT} \simeq N_D$$

$$\frac{N_c}{N_D} = e^{E_c - E_F/KT}$$

$$\log_e \frac{N_c}{N_D} = \frac{E_c - E_F}{KT}$$

$$E_c - E_F = KT \log_e \frac{N_c}{N_D}$$

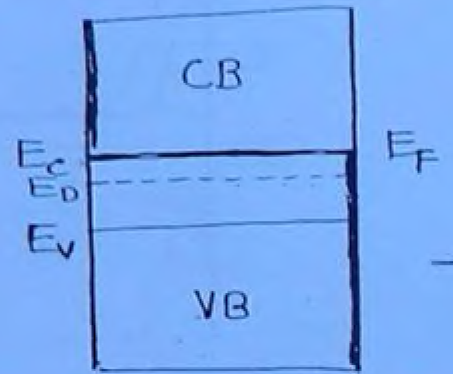
$$E_F = E_c - KT \log_e \frac{N_c}{N_D}$$

⇒ In N-type SC fermi level depends on temp and doping conc^n

Case-I

At T=0K.

$$E_F = E_C$$



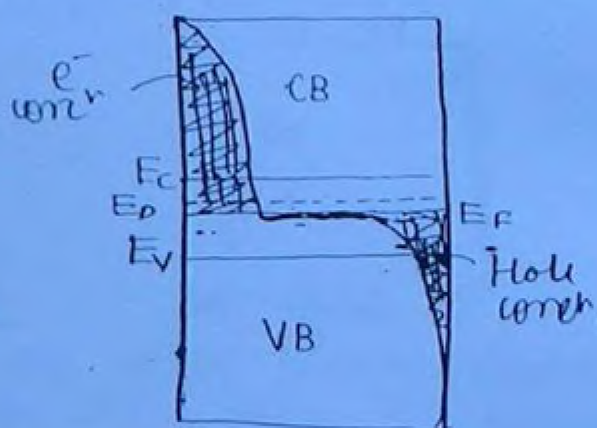
⇒ E_F coincides E_C

⇒ At 0K carrier conc^n are zero and therefore conductivity is zero and N-type SC will behave as insulator.

Case-II

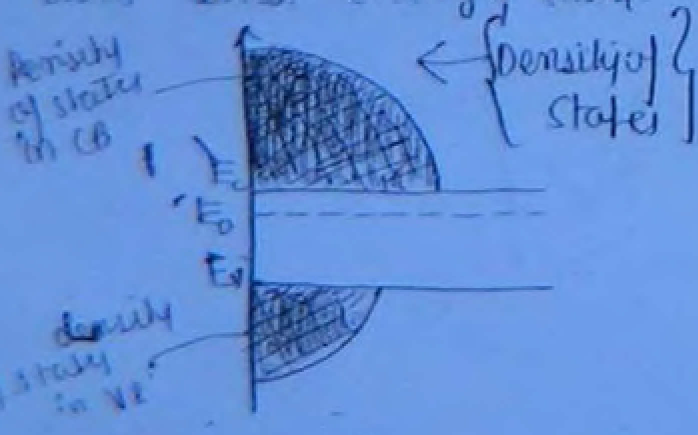
At T = 300K

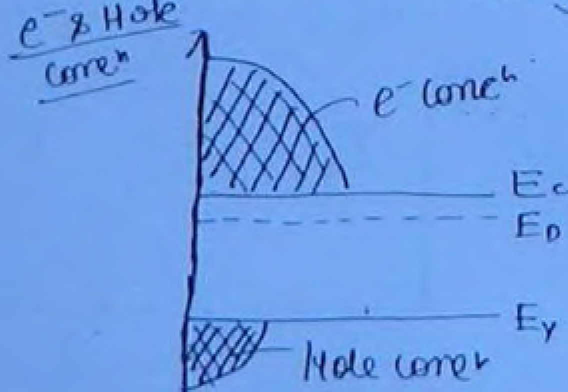
$$E_F = E_C - KT \log_e \frac{N_C}{N_D}$$



⇒ In N-type SC at room temp fermi level exists just below the Donor energy level.

⇒ As temp is increasing from 0K to 300K at some intermediate temp the fermi level will be coinciding with donor energy level.





Case III Formation :

$$E_c - E_F = KT \log_e \frac{N_c}{N_D}$$

(i) Let T ⇒ Increases :→

$N_c \uparrow$ & let $N_c > N_D$

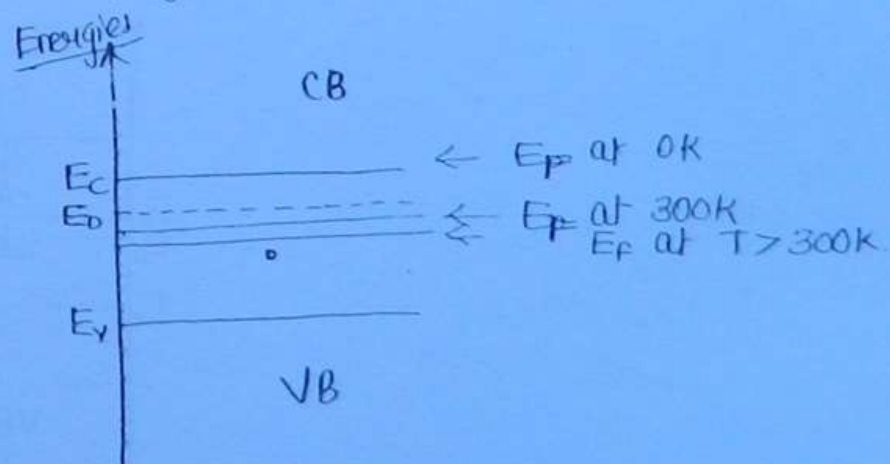
$E_c - E_F > 0$

$\Rightarrow$ $\boxed{E_c > E_F}$

→ T ↑ in N-type SC fermi level moves away from CB (or)

→ Fermi level moves towards the centre of energy gap. Hence conductivity decreases with temperature.

→ The position of fermi level for different temp for N-type SC is given below :→



⇒ At curie temperature E_F will be existing at the centre of energy gap.

⇒

(ii) Let Doping ↑ :⟹

$N_D \uparrow$ and $N_D > N_c$

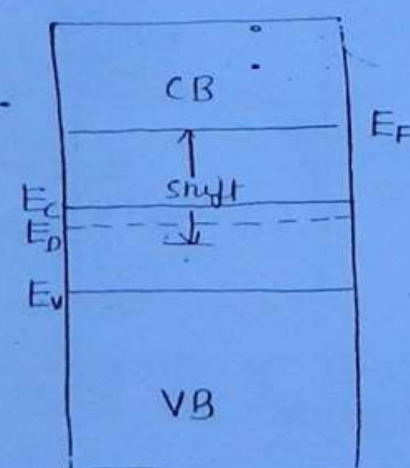
$E_c - E_F < 0$

$\Rightarrow \boxed{E_c < E_F}$

⟹ In N-type SC Doping ↑ (N_D) fermi level moves into the conduction band or moving away from the centre of energy gap.
Hence σ will increases with doping ↑.

⟹ In N-type SC as Doping increases, E_F takes upward shift.

⟹ In a Highly Doped N-type SC or Highly degenerated N-type SC, the E_F exist in CB.



Case IV

Shift in the position of fermi level due to Doping.

(Or)

Shift in the position of E_F w.r.t E_F of Intrinsic SC.

(Or)

Shift in position of E_F w.r.t to centre of energy gap.

$$\Rightarrow \boxed{\text{Shift} = kT \log_e \frac{N_D}{n_i}} \text{ eV.}$$

$$\Rightarrow \boxed{\text{Shift} = kT \log_e \frac{n}{n_i}} \text{ eV}$$

Fermi-level in p-type Semiconductor :→

$$p \simeq N_A$$

$$N_V e^{-[E_F - E_V]/KT} = N_A$$

$$\frac{N_V}{N_A} = e^{E_F - E_V/KT}$$

$$\frac{E_F - E_V}{KT} = \log_e \frac{N_V}{N_A}$$

$$\Rightarrow \boxed{E_F - E_V = KT \log_e \frac{N_V}{N_A}}$$

$$\Rightarrow \boxed{E_F = E_V + KT \log_e \frac{N_V}{N_A}}$$

→ In p-type SC fermi-level depends on temp. and doping concⁿ

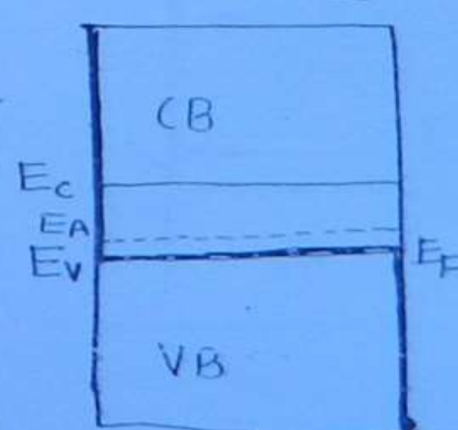
Case I :→

let T = 0 K

$$\boxed{E_F = E_V}$$

E_F coincides with E_V

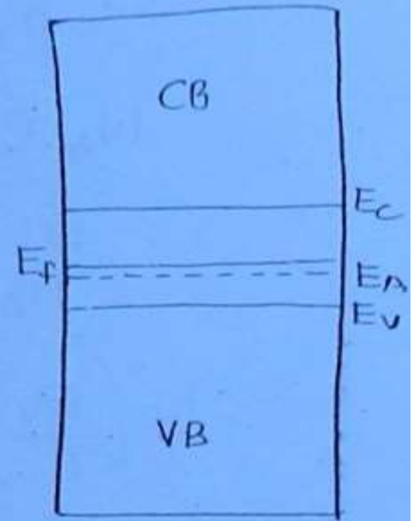
At T=0K



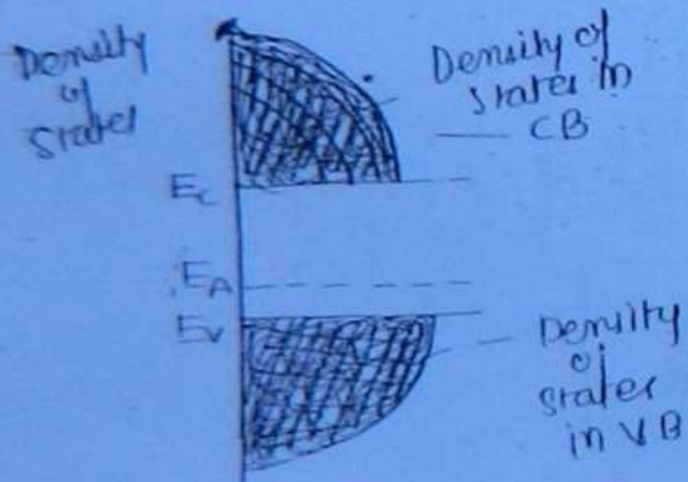
⇒ At 0K carrier concⁿ are zero and therefore conductivity is zero. and therefore p-type SC at 0K behaves as insulator

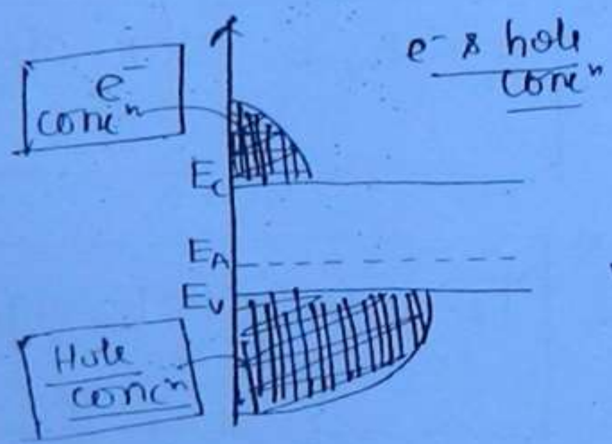
Case II → let T = 300K

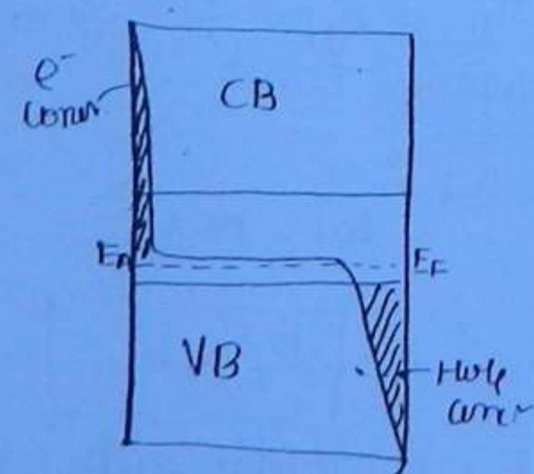
$$E_F = E_V + kT \log \frac{N_V}{N_A}$$



⇒ In P-type semiconductor at room temp. fermi-level is existing just above the acceptor energy level







Case III

$$E_F - E_V = KT \log_e \frac{N_V}{N_A}$$

(i) let Temp ↑

N_V ↑ and let $N_V > N_A$

$E_F - E_V > 0$

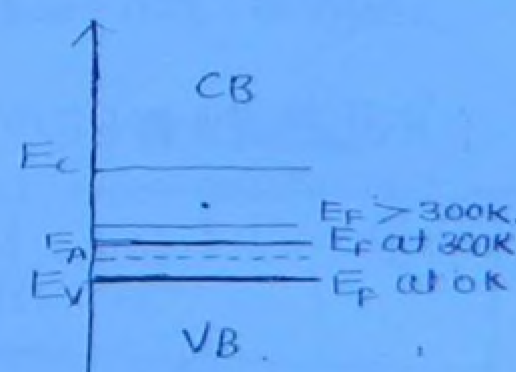
$\Rightarrow$ $E_F > E_V$

→ In P-type SC Temp ↑ E_F moves away from VB or E_F moves towards the centre of energy gap

$\Rightarrow$ ∴ σ ↓ with temp ↑

→ In P-type SC the position of fermi-level for different temperature is given below

→ At curie temperature, the fermi level will be at the centre of the energy gap



(ii) let Doping concⁿ ↑

N_A ↑ & let $N_A > N_V$

$E_F - E_V < 0$

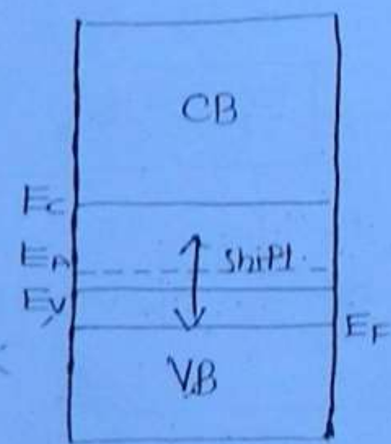
$\Rightarrow$ $E_F < E_V$

→ In P-type SC as doping ↑ E_F moves into the VB. or E_F away from the centre of energy gap.

$\Rightarrow$ ∴ σ ↑ with doping ↑

→ In P-type SC as doping increases fermi-level takes downward shift. (denoted with -ve sign)

→ In a highly doped p-type SC or highly degenerated p-type SC, the fermi level will exists in the VB.



P SC at 300K

Case IV Shift in the position of fermi level due to Doping

or

Shift in the position of E_F w.r.t. E_F of intrinsic SC.

or

Shift in the position of E_F w.r.t centre of energy gap.

$$\Rightarrow \boxed{\text{Shift} = KT \log_e \frac{N_A}{n_i}} \text{ eV}$$

(or)

$$\boxed{\text{Shift} = KT \log_e \frac{P}{n_i}} \text{ eV}$$

↑ downward

Prob. In a N-type SC, the fermi level lies 0.3 eV below the CB at 300K if the temp is increased to 330K find the approximate new position of fermi level.

Soln N-type SC

$$E_c - E_F = KT \log_e \frac{N_c}{N_D}$$

$$E_c - E_F \propto T$$

$$E_c - E_F \propto \log \frac{N_c}{N_D}$$

neglecting the variation of N_c with temp

$$E_c - E_F \propto T.$$

$$0.3 \propto 300K$$

$$E_c - E_{F2} \propto 330$$

$$\therefore E_c - E_{F2} = \frac{330}{300} \times 0.3 = 0.33\ eV.$$

Prob In N-type SC, the E_F lies 0.4 eV below CB if the concn of N_D is doubled find New position of E_F. Assume $KT = 0.03$ eV.

Soln

$$N_D = N_c e^{-(E_c - E_F)/KT}$$

$$N_D = N_c e^{-0.4/0.03} \rightarrow (1).$$

$$2N_D = N_c e^{-(E_c - E_{F2})/0.03} \rightarrow (2)$$

$$\frac{1}{2} = \frac{e^{-0.4/0.03}}{e^{-(E_c - E_{F2})/0.03}}$$

$$\frac{1}{2} = e^{-0.4/0.03 + (E_c - E_{F2})/0.03} \Rightarrow \frac{-0.4}{0.03} + \frac{E_c - E_{F2}}{0.03} = \log_e\left(\frac{1}{2}\right)$$

$$\Rightarrow E_c - E_{F2} = 0.4 + 0.03 \log_e \frac{1}{2} \Rightarrow 0.37\ eV.$$

Q8 For P-type SC the fermi level lies 0.4 eV above the VB if conc^n of acceptor atoms is tripled find New position of E_F. Assume $KT = 0.03$ eV

(0.367 eV)

$$N_A = N_V \, e^{(E_F - E_V)/KT}$$

$$N_A =$$

Prob · In a SC at room temp, the intrinsic carrier conc^n and intrinsic resistivity are $1.5\times10^{16}/m^3$ & $2\times10^{13}\ \Omega$-m resp. It is converted into an extrinsic semiconductor with doping conc^n of $10^{20}/m^3$. Find the shift in the E_F due to doping.

Sol^n

$$n_i = 1.5\times10^{16}/m^3$$

$$\rho_i = 2\times10^{13}\ \Omega\text{-m}$$

$$\text{Doping conc}^n = 10^{20}/m^3$$

$$\text{Shift} = KT \log_e \frac{\text{Doping conc}^n}{n_i}\ eV$$

$$= 8.62\times10^{-5}\times300\ \log_e \frac{10^{20}}{1.5\times10^{16}}$$

$$\Rightarrow \boxed{\text{Shift} = 0.227\ eV}$$

Prob Si is doped with B to a conc^n of 4×10^{17} Atoms/cm^3. Assume $n_i = 1.5\times10^{10}/cm^3$ & $T = 300K$. Compare to undoped Si the doped, the fermi level of doped Si is ______

Sol^n

$$\left.\begin{matrix} n_i = 1.5\times10^{10}/cm^3 \\ N_A = 4\times10^{17}/cm^3 \end{matrix}\right\} \quad \underline{\text{P-type}}$$

$$\text{Shift} = 8.62\times10^{-5}\times300\ \log_e \frac{4\times10^{17}}{1.5\times10^{10}}$$

$$\text{Shift} = 0.44\ eV$$

In P-type SC E_F takes downward shift of 0.44eV

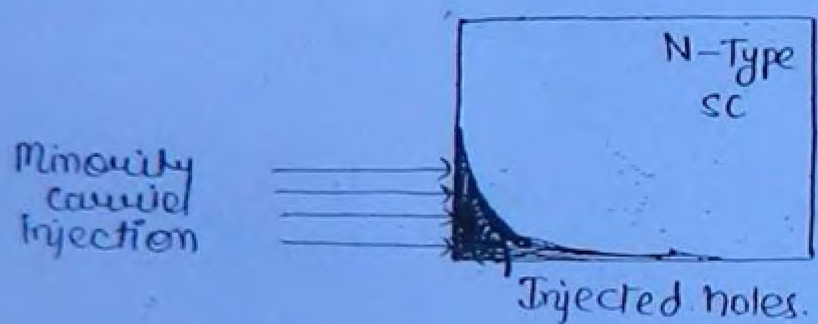
$$\boxed{\text{Shift} = -0.44\ eV} \quad \text{Ac}$$

⟹ Low Level Injection

→ It means the conc^n of majority carrier conc^n is far greater then minority carrier conc^n.

→ Under low level injection light is focused on semiconductor.

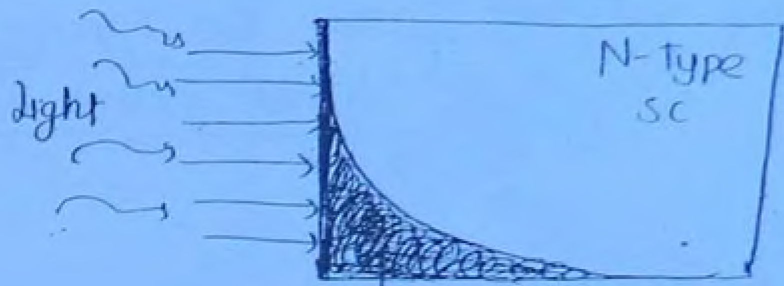
→ Minority Carrier Injection into SC



→ When minority carrier are injected into the semiconductor bar, the injected minority carrier conc^n will be maximum at the surface where it is introduced into the semiconductor and the injected minority carrier conc^n will be moving in the semiconductor from higher conc^n to lower conc^n i.e. due to the <u>diffusion mechanism</u>

→ When hole is introduced into the N-type SC bar the injected hole will be moving in the SC from higher conc^n to lower conc^n i.e due to property called diffusion

When light falls on a SC :→ {For Grade ONLY very imp}



Injected holes in N-type SC.

→ Light is focused on the SC under low level injection

→ A light falls on SC, because of photon energy the surface of the SC gets heated up and due to this thermal energy a no. of covalent bond will be broken creating equal no of e^- and equal no. of holes

→ Under steady state condⁿ excess e^- generated is equal excess holes generated i.e.

$$\Rightarrow \boxed{\Delta n \equiv \Delta p}$$

→ The injected minority carrier concⁿ will be maximum on the surface of the SC where light is focussed and the injected minority carrier concⁿ will be moving in the SC from higher concⁿ to lower concⁿ i.e. due to the diffusion mechanism

→ The generation rate or generation of e^- hole pair is given by :→

$$\Rightarrow \boxed{\frac{dp}{dt} = \frac{\text{Excess holes generated}}{\text{minority carrier life time}}}$$

$$\rightarrow \boxed{\frac{dp}{dt} = \frac{\Delta p}{\tau_p} \; e^- \text{ hole pairs/cm}^3\text{/sec}}$$

Prob. Generation rate due to irradiation in N-type SC having $N_D = 10^{17}/cm^3$ when excess e^- concⁿ in steady state is $\Delta n = 10^{15}/cm^3$ and $\tau_p = 10\mu sec$.

{Gate exam imp.}

soln Generation rate $= \Delta p / \tau_p$

$\Delta p \equiv \Delta n$

$\Delta p = 10^{15}/cm^3$

Generation rate $= \dfrac{10^{15}}{10 \times 10^{-6}} = 10^{20}$ e^- hole pair/cm³/sec

→ **considering N-type SC and light is focussed**

→ when light falls on a SC, minority carriers are generated.

→ when light is focussed on N-type SC, there will be two current component in the SC & they are
- hole diffusion current (because of photon energy)
- hole drift current (because of doping profile)

→ under low level injection ~~minorit~~ hole drift current is almost negligable.

→ under low level injection current in the SC is dominated by diffusion.

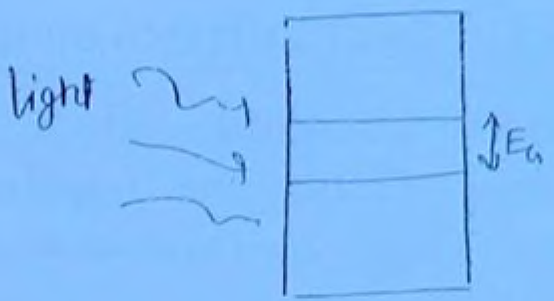
Wavelength of light

→ $\lambda = \dfrac{1.24}{E_G}$ μm E_G → Energy gap of material in eV

→ wavelength of visible light is in range of 0.38 μm to 0.76 μm

→ if wavelength > 0.76, it belong to infrared region.

Intrinsic Excitation :→



if photon energy $\geq E_G$

i.e.

$$h\nu \geq E_G$$

→ Electron may be exciting from VB to CB

→ When light falls on SC, an e^- may be exciting from VB to CB & this called intrinsic excitation.

→ The minimum photon energy required for intrinsic excitation is equal to E_G

Extrinsic Excitation

→ When light falls on N-type SC, an e^- may be exciting from donor energy level into the conduction band & this is called extrinsic excitation

→ When light falls on P-type SC, an e^- may be exciting from valency band into acceptor energy level and this is called extrinsic excitation.

→ The minimum photon energy required for extrinsic excitation $\begin{cases} 0.01 \text{ eV for Ge} \\ 0.05 \text{ eV for Si} \end{cases}$

DIODE

PHOTOCONDUCTIVE Effect :→

→ It is the property where the conductivity of a material or device increases with the light is called photoconductive effect.

→ Photoconductive effect is sometimes called photo-resistive effect.

→ The property where the resistivity of material or device decreases with the light is called photo-resistive effect.

SEMICONDUCTOR DIODE

P-N junction diode

→ Rectification properties are existing.

→ Can be used as rectifier

Metal SC Junction dio

→ No such properties

→ Cannot work as rectifie

e.g. ① Shottky Diode

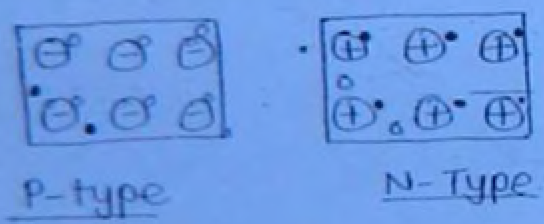
② Point contact Dio

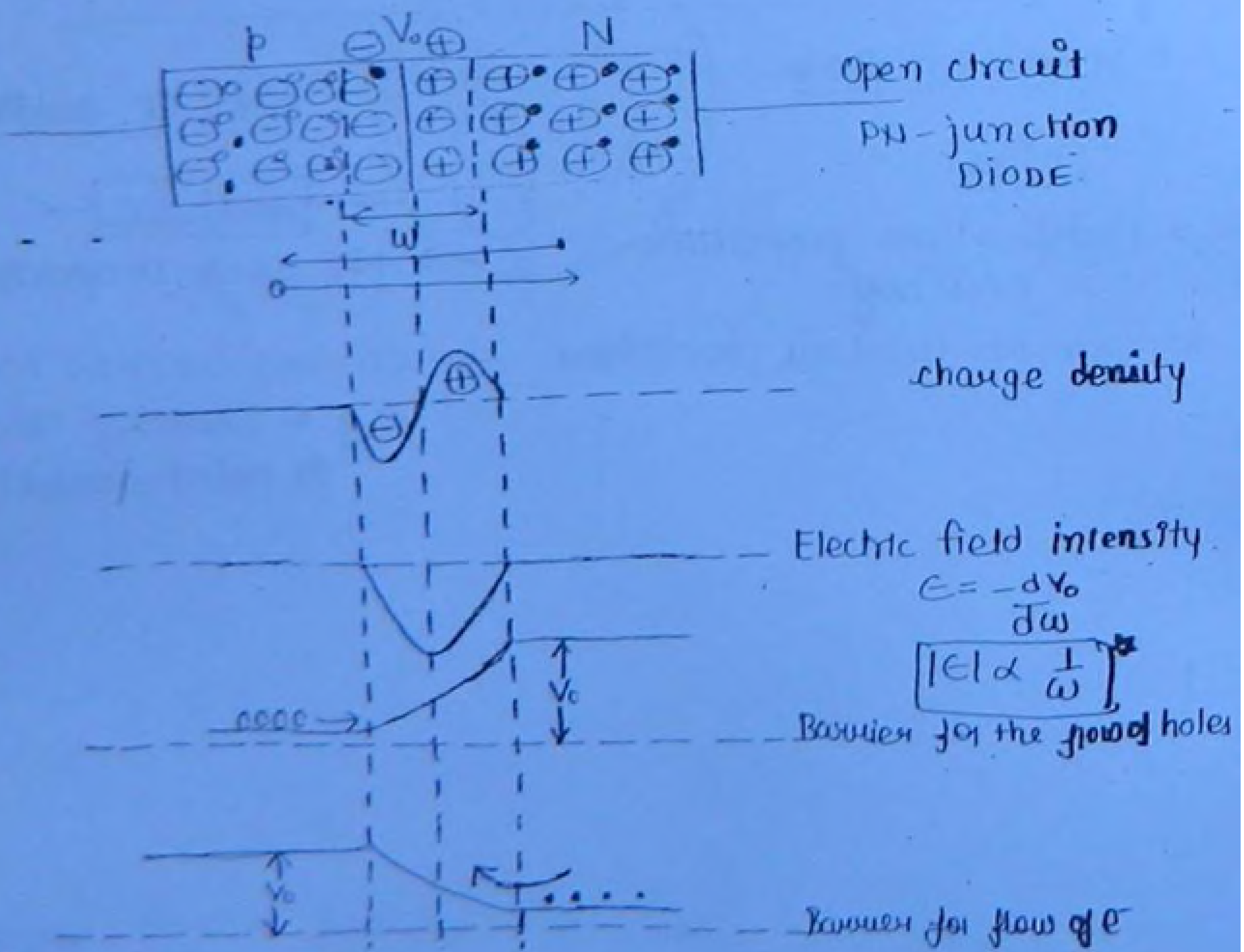
P-N-Junction Diode

→ A p-n-junction will formed only when a bonding force is created inbetween the p-type and N-type semiconductors.

→ Diodes are fabricated by using :→

(1) Alloy-Junction Technique
(2) Grown-junction Technique
(3) Epitaxial method.
(4) Diffusion method.





→ Depletion layer is also called space charge region or transition region.

→ Depletion layer is created due to diffusion of majority carriers across the junction.

→ Depletion layer width

$$\omega \propto \frac{1}{\sqrt{Doping}}$$

→ W is the range of 0.1 μm to 1 μm.

→ Typical value of W is 0.5 μm

→ In the Depletion layer mobile charge carrier are zero.

→ Depletion layer consist of ions and covalent bonds

→ Depletion layer consist of immobile charged particles.

→ Depletion layer consist of negative and positive charges on the either side of the junction.

→ Depletion layer consist of negative ions (acceptor ions on the p-side) and positive ions (donor ions on the N-side).

→ Depletion layer will oppose the majority carrier in crossing the junction

→ Depletion layer will not oppose minority carriers in crossing the junction

→ Depletion layer will help minority carrier in crossing the junction.

→ Depletion layer is extremely narrow where doping concn is very high

→ V_0 is called potential hill or contact potential or barrier potential or diffusion voltage or Built in voltage (V_{bi}).

→ <u>For Ge diode</u>

$V_0 = 0.1V$ to $0.5V$

and Typical value $0.2V$

<u>For Si Diode</u>

$V_0 = 0.6V$ to $0.9V$

& Typical value $0.7V$

→ Contact potential of diode cannot be practically measured by using a voltmeter.

→ In any type of P-N junction, the field intensity is always maximum at the junction

→ In a normal diode, field intensity is negative and it is maximum at the junction and it tappers on eigther side of junction and it is zero outside the Depletion layer.

→ Majority carriers will be climbing up the barrier voltage and therefore there will be an opposition

→ Minority carriers will be falling down the barrier voltage and therefore there will no opposition for the minority carriers.

SYMBOL

→ The arrow mark on diode symbol denotes the direction of forward current.

→ **Equation for width of Depletion layer in OC Dio**

$$W = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)V_0} \text{ metres}$$

ε = Permitivity in F/m = $\epsilon_0 \epsilon_r$.

ϵ_0 = Absolute permittivity of free space.

$\epsilon_0 = 8.854 \times 10^{-12}$ F/m

ϵ_r = Relative permittivity of medium.

* { ϵ_r for Si = 11.7 ; ϵ_r for Ge = 16 }

→ The width of Depletion layer in OC diode depends on :-

1. Doping conc^n of P-N region.
2. Contact potential of diode
3. Relative permitivity of medium.

Assume $N_A = N_D$

$$W = \sqrt{\frac{2\epsilon}{q}\left(\frac{2}{N_A \text{ or } N_D}\right)} \Rightarrow \boxed{W \propto \frac{1}{\sqrt{\text{Doping}}}}$$

Contact Potential in OC P-N-junction.

$$V_0 = V_{bi} = V_T \log_e \frac{N_A N_D}{n_i^2} \text{ volts}$$

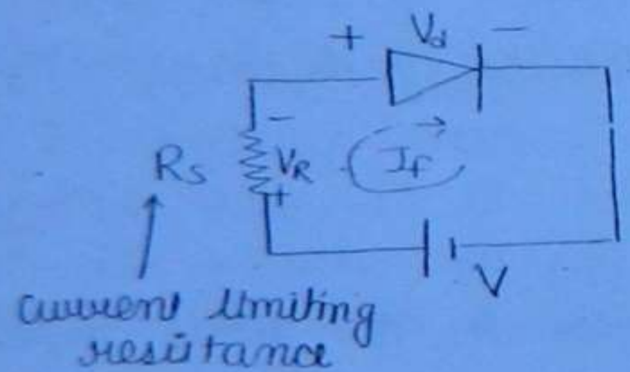
→ Contact potential of diode depends on:-

① Doping concn of P & N region

② Temperature.

→ In OC p-N-junction, if doping concn are increased can contact potential of diode slightly increases.

FORWARD BIASED



$$W \propto \frac{1}{\sqrt{F.B.}}$$

$$V = V_R + V_d$$

$$V = I_f R_s + I_f R_f$$

→ When a P-N junction is FB, the width of depletion layer decreases and also the barrier height reduces.

NOTE :→ In a FB P-N junction the effect of barrier is nullified i.e. the barrier voltage will not oppose the majority in crossing the junction

→ Forward current is only due to majority carrier:

$$I_f = I_0 \left[e^{\frac{V_d}{\eta V_T}} - 1 \right] \text{ Amp}$$

$$\Rightarrow \boxed{I_f \approx I_0 \, e^{\frac{V_d}{\eta V_T}}} \text{ Amp.}$$

→ V_T is thermal voltage (26 mV)

V_d forward voltage across the diode (below 0.5 V for Ge, 0.9 V for Si)

η is called recombination factor or utility factor

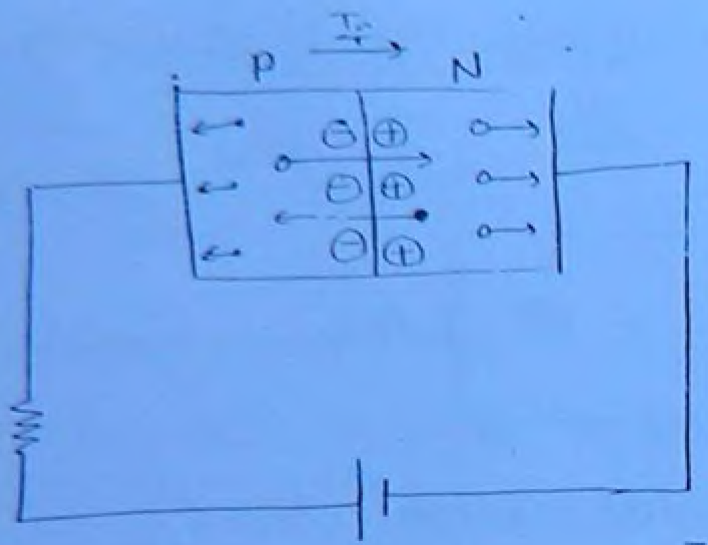
$\eta = 1$ for Ge or for larger current
$\quad 2$ for Si or for smaller current

→ In the given problem of Ge & Si is not specified then by default $\eta = 1$.

I_0 is reverse saturation current or minority carrier current.

→ Forward current is only due to majority carrier but it is mathematically derive in terms of minority carrier current.

→ Forward current exponentially increases with forward voltage across the diode.



→ Forward current flows from P to N.

→ Forward current is large (mA)

→ In forward biased diode the minority carrier will be moving away from the junction and they will not contribute any current.

→ Forward current is a diffusion current.

→ Forward current is only due to majority carrier and majority carriers are crossing the junction from higher to lower concⁿ i.e. due to property called diffusion. Hence forward current is diffusion current.

→ **Cutin Voltage V_γ**

→ Also called offset Voltage or threshold voltage or knee voltage or break voltage.

→ It is defined as the minimum forward voltage above which the current flows in the diode.

For Ge Diode

$V_\gamma = 0.1\ V$ to $0.5\ V$ $(0.2\ V)$

For Si Diode

$V_\gamma = 0.6\ V$ to $0.9\ V$ $(0.7\ V)$

★ Cutin voltage decreases with temperature.

★ { For 1°C $V_\gamma \downarrow$ by 2.3 mV (latest) or 2.5 mV (old) }

Effect of temperature on Forward current

- Forward current of diode is independent of temperature.
- Forward current is due to majority and majority carrier concⁿ is independent of temperature

FORWARD Voltage Across the Diode, V_d

$$\Rightarrow V_d = \eta V_T \log_e \left(\frac{I_f}{I_o} \right)$$

- Between V_T & I_o, I_o is more sensitive to the temperature
- Voltage drop (V_D) decreases with the temp.

★ { For 1°C $V_D \downarrow$ 2 mV (latest) or 2.5 mV (old) } ★

- A forward biased diode is subjected to a temperature variation of 10°C then the forward voltage of diode changes by 20 mV.

REVERSE BIAS

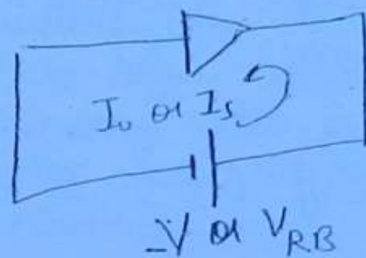
or

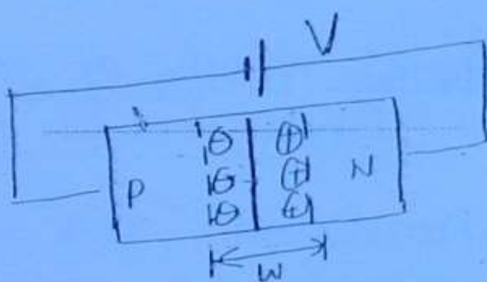
Blocking Bias

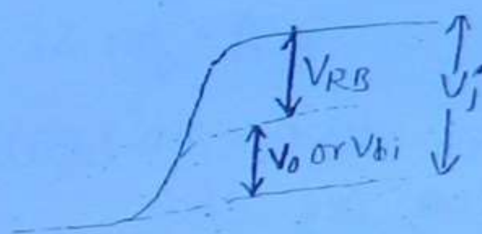
or

Back Bias.

→







Junction Voltage V_j = sum of V_{bi} & V_{RB}

$$V_j = V_{bi} + V_{RB}$$

Width of depletion layer $w \propto \sqrt{V_j}$

$$w \propto \sqrt{V_{bi} + V_{RB}}$$

if V_{bi} is neglected

$$V_j \approx V_{RB}$$

$$\therefore\ w \propto \sqrt{\text{RB voltage}}$$

When P-N junction is RB the width of the depletion layer increases and also the barrier height increases.

→ The Reverse current I_0 is called Thermally generated current or leakage current or reverse saturation current.

→ $I_0 = \mu A$ for Ge, nA for Si } I_0 of Ge > I_0 of Si

→ Si diode is having better thermal stability then Ge diode

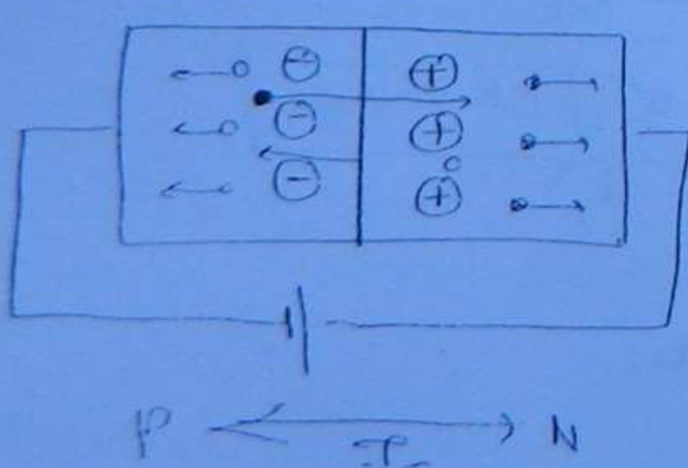
→ I_0 flows from N to P.

→ I_0 is independent of applied voltage (this current is saturated with respect to applied voltage)

→ For 1°C I_0 approx increases by 7%

→ For 10°C I_0 will becomes doubles :-

$$I_0(T_2) = I_0(T_1)\left[2^{\frac{T_2-T_1}{10}}\right]$$



In a RB PN junction, the majority carriers will be moving away from the junction and therefore they will not be contribute any current.

→ Reverse current is a drift current

→ Reverse current is due to minority carrier and this minority carriers are crossing the junction from low concⁿ to high concⁿ or the minority carrier will be crossing the junction due to electric field intensity and therefore a reverse current is a drift current.

Equation for width of Depletion layer in Reverse Biased Diode

In RB P-N Junction

$$W = \sqrt{\frac{2\epsilon}{q}\left(\frac{1}{N_A} + \frac{1}{N_B}\right)(V_D + V_{RB})}$$

$$W \propto \sqrt{V_{bi} + V_{RB}} \quad \text{or} \quad W \propto \sqrt{V_j}$$

→ Majority carriers are blocked in crossing the junction and therefore it is called blocking Bias

Equation for current I in a RB Diode :→

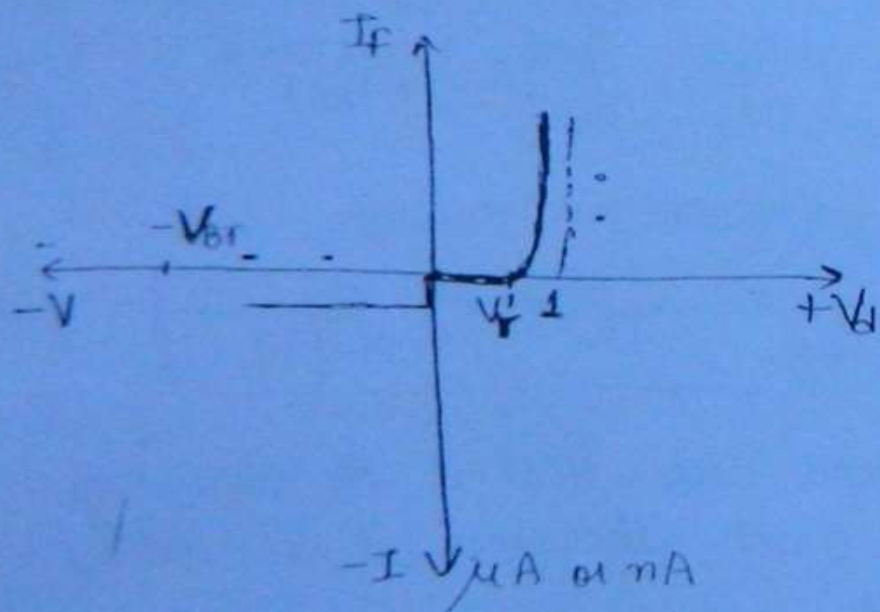
$$\Rightarrow \boxed{I = I_0}$$

$$\Rightarrow \boxed{I = -I_0 \left[e^{-V/nV_T} - 1 \right]}$$

V-I CHARACTERISTCS OF DIODE

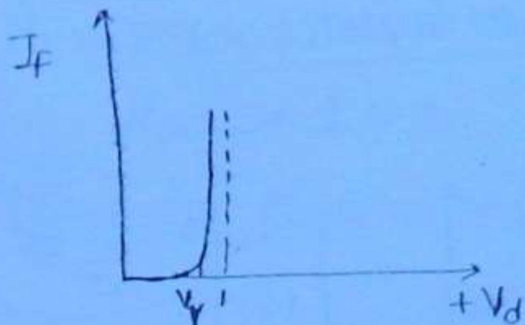
or

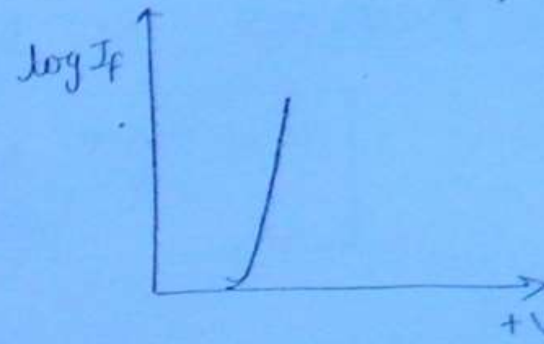
Volt-Amphere characteristics of Diode.



$$\text{Slope} = \frac{I_F}{V_d} = \frac{1}{V_d / I_F} = \frac{1}{R_f}$$

→ When a normal diode is reverse biased the reverse voltage must be less then breakdown voltage of the device otherwise the diode will be destroyed



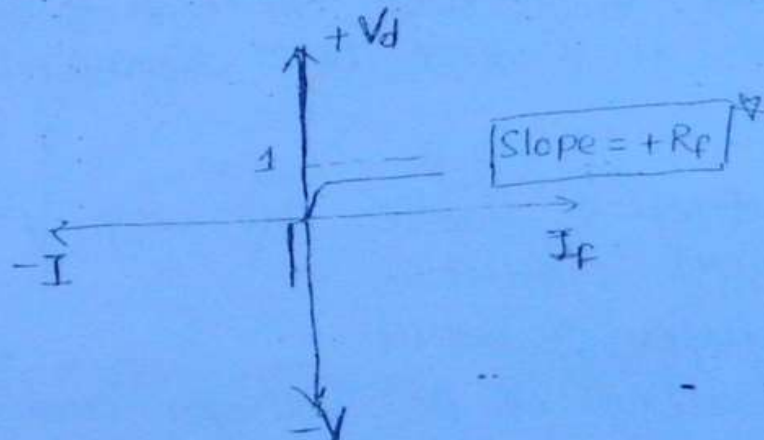


{ I_F exponentially ↑ with V_d }

{ $\log I_F$ vs V_d curve represents a st. line }

→ For increasing curve slope is positive and +ve

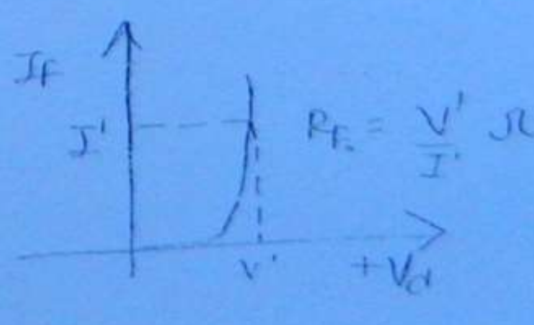
IV characteristics



Diode Resistance

↓
Forward Resistance
10 Ω to 100 Ω

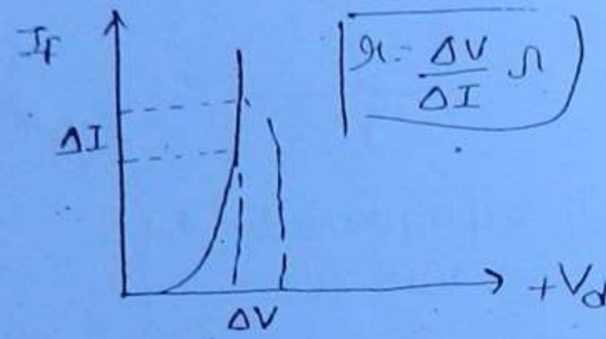
↓
DC Resistance
or
Static Resistance
↓ 'R_F'



It is resistance of diode when '0' input signal is applied or resistance of diod under

→ AC Resistance or Dynamic Resistance

$$r = \frac{\Delta V}{\Delta I} \, \Omega$$



→ It is the resistance of diode when signal is applied i.e. under A.C. Analysis

⇒ D.C resistance is greater then A.C resistance (static resistance is greater then Dynamic resistance

→ Under DC analysis of diode, All signal voltages are short circuited

→ Under AC analysis of diode

- → Biasing voltages or DC voltages are SC.
- → The Diode is replaced by its Dynamic resistance

REVERSE Resistance.

$R_r > 1 M\Omega$

Dynamic Resistance of Diode

$$\Rightarrow \boxed{r = \frac{\eta V_T}{I_f}}$$

At 300K, if $I_f = 26mA$

For Ge Diode, $r = 1\Omega$.
Si Diode, $r = 2\Omega$.

when compared to germanium diode Si diode has larger dynamic resistance.

$$\Rightarrow \boxed{r = \frac{\eta V_T}{I_f} = \frac{\eta KT}{q I_f}}$$

Dynamic Conductance of diode (g): →

$$\boxed{g = \frac{1}{r} \quad \text{Ʊ or S or A/V}}$$

$$\boxed{g = \frac{I_f}{\eta V_T}}$$

$$\boxed{g \propto I_f}$$

$$\Rightarrow \boxed{g = \frac{q I_f}{\eta KT}}$$

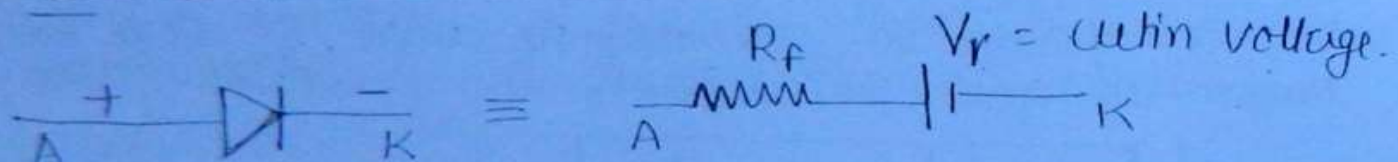
Breakdown Voltage [V_{Br} or Br] :⟹

→ In any type of PN junction breakdown voltage

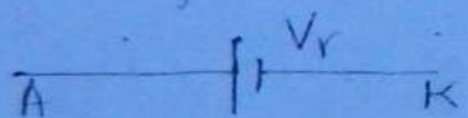
☆☆ ⟹ $$V_{Br} \propto \frac{1}{\text{Doping}}$$

Equivalent Circuit of Diode ⟹

1) **When diode is FB :→**

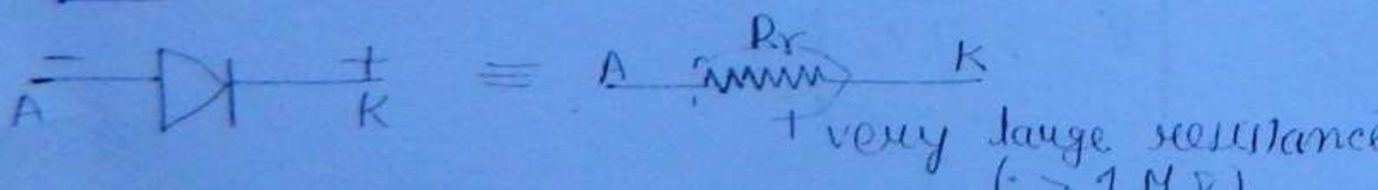


→ Supposing forward Resistance of diode is zero or not given then



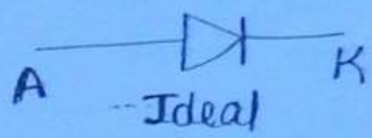
→ A FB Diode can be replaced by its cutin voltage

2) **When diode is RB :→**



IDEAL DIODE ⇒
or
Perfect Diode or Imaginary Diode :→

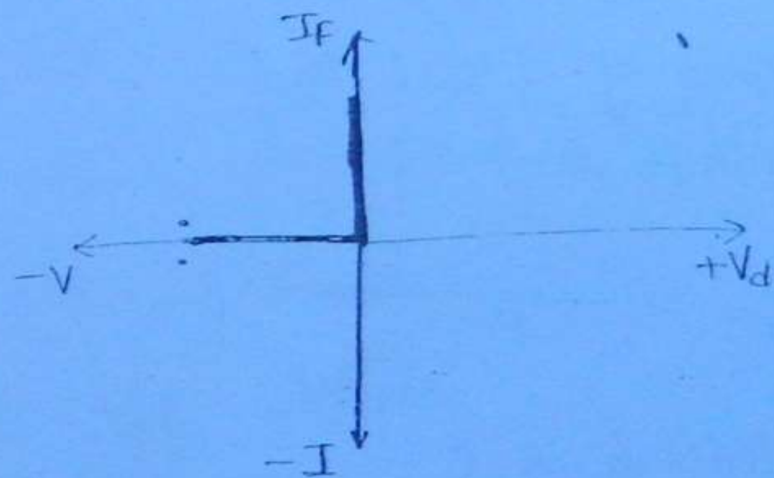
Symbol :→



Properties :-

$$\left\{ \begin{array}{l} R_f = 0 \\ R_r = \infty \\ V_\gamma = 0 \end{array} \right\}$$

VI characteristics



if Ideal diode is FB
It is SC
$I \rightarrow max.$
$V \rightarrow 0$

if ID is RB
It is OC
$I = 0$
$V \rightarrow max$

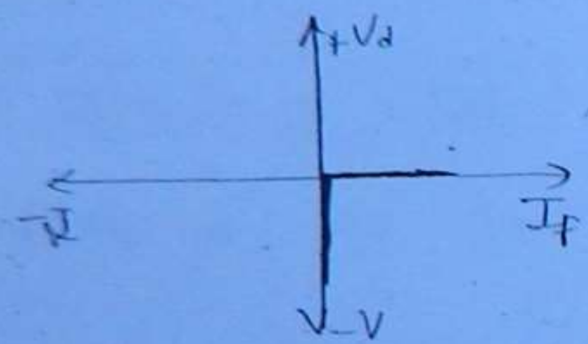
→ When Ideal diode is FB, it is treated as SC

∴ $R_f = 0$

→ when ideal diode is RB it is treated as OC.

∴ $R_r = \infty$

IV characteristics



Equivalent Circuit of Ideal diode

(i) when Ideal Diode in FB :-

(ii) when ideal diode is RB :-

Prob. Find the forward current of a Ge diode operating at room temperature with a forward voltage of 100 mV across it. The reverse saturation current 20 μA.

soln

$$I_F = I_0 \, e^{V_d/\eta V_T}$$

$$I_F = 20 \times 10^{-6} \, e^{\frac{100mV}{260}}$$

$$\boxed{I_F = 0.936 \, mA}$$

Prob. A Si Diode operating at room temp. with forward voltage of 650mV and having a likeage current 20 nA. find its Dynamic resistance.

soln

$$I_F = I_0 \, e^{V_d/\eta V_T}$$

$$I_F = 20 \times 10^{-9} \, e^{\frac{650 \times 10^{-3}}{2 \times 26 \times 10^{-3}}}$$

$$I_F = 5.367 \, mA$$

$$\Rightarrow r = \frac{\eta V_T}{I_F}$$

$$\Rightarrow r = \frac{2 \times 26}{5.367}$$

$$\Rightarrow \boxed{r = 9.688 \, \Omega}$$

Prob A diode has a leakage current of 10μA at certain temperature. find its value when temp. is increased by 25°C ?.

Soln

$$I_{02} = I_{01}\left[2^{\frac{T_2 - T_1}{10}} \right]$$

$$= 10\mu A \left[2^{\frac{T_1 + 25 - T_1}{10}} \right]$$

$$= 10\mu A \left[2^{2.5} \right]$$

$$\Rightarrow \boxed{I_{02} = 56.56\mu A}$$

Prob A step graded Ge diode having $N_D = 500 N_A$. Acceptor impurities to extent of $2 : 10^8$ is added at room temp. find its contact potential. Assume $n_i = 2.5 \times 10^{13}$ atom/cm³. Total no. of atoms $= 4.421 \times 10^{22}/cm^3$

Soln

$$V_o = V_T \log_e \frac{N_A N_D}{n_i^2}$$

$$N_A = 4.421 \times 10^{22} \times \frac{2}{10^8} = 8.842 \times 10^{14}$$

$$V_o = 26 \times 10^{-3} \log_e \frac{8.842 \times 10^{14} \times 500 \times 8.842 \times 10^{14}}{(2.5 \times 10^{13})^2}$$

$$V_o = 26 \times 10^{-3} \log_e \frac{3.90 \times 10^{32}}{6.25 \times 10^{26}}$$

$$V_o = 26 \times 10^{-3} \log_e 624000 \rightarrow 0.347V$$

Prob A step graded Si diode having $N_D = 500 N_A$ the acceptor impurities $\lambda : 10^8$ are added at room temperature find its contact potential

Assume $n_i = 1.5 \times 10^{10}$

Total no. of atoms $= 5 \times 10^{22}$ atom/cm^3.

$$\boxed{V_0 = 739\ mV}$$ Ans

Qust A Si Diode Indicates forward current of 2mA and 10mA when diode voltages are 0.6V and 0.7V resp. Estimate the operating temperature of the diode junction.

Soln

$$I_F \approx I_0 e^{V_d/\eta V_T}$$

but $V_T = T/11600$

$$\Rightarrow \boxed{I_F = I_0 e^{\frac{11600 V_d}{\eta T}}}$$

$$\frac{2mA}{10mA} = \frac{e^{\frac{11600(0.6)}{2T}}}{e^{\frac{11600(0.7)}{2T}}}$$

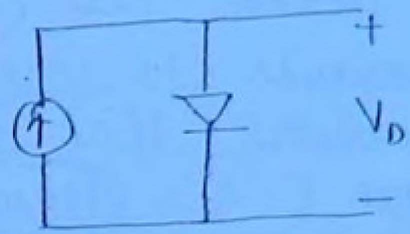
$$\frac{1}{5} \approx e^{\frac{11600(0.6)}{2T} - \frac{11600(0.7)}{2T}}$$

$$\frac{1}{5} \approx e^{-580/T}$$

$$T = \frac{-580}{\log\left(\frac{1}{5}\right)}$$

$$\Rightarrow = +360^\circ K$$

Prob: In the circuit given below, Si diode is carrying a const. current of 1 mA.



when temperature of diode is 20°C, V_D is formed to be forward voltage across diode is 700 mV if temp increases to 40°C then V_D becomes equal to ________

soln: Temp. ↑ from 20°C to 40°C

$\Delta T = 20°C$

$1°C, \quad V_D \downarrow \quad 2\,mV$

$20°C \quad \Delta V_D \downarrow \quad \frac{2\,mV}{°C} \times 20\,mV$

$\Delta V_D = 40\,mV$

$V_D = 700\,mV - \Delta V_D$

$= 700 - 40 = 660\,mV$. Ans

Prob: A FB Si Diode when carrying negligable current as a voltage drop of 0.64 V when current is 1 A it dissipates 1 watt. ON resistance of diode is 1Ω

soln: $I = 1\,A$

$P = 1\,W$

$P = I^2 R$

$R_{ON} = 1\Omega$ Ans.

Prob A pn junction in series with a 100Ω resistor is FB so that a current of 100mA flows if the voltage across this combination is instantaneously reverse to 10V at time t=0. The reverse current that flows through diode at time t=0 (100mA)

Soln → At time t=0, the diode is still under forward biased and the current in the circuit is (100mA) Ans.

Prob At 300K, for a diode current of 1mA, a certain Ge diode requires a FB of 0.1435V across it whereas Si diode requires FB of 0.718V across it. Under condn given above find ratio of $I_0(Ge)/I_0(Si)$

Soln

$$\frac{I_{0(Ge)}}{I_{0(Si)}} = ?$$

$$I = I_0 e^{V_f/\eta V_T}$$

For Ge

$$1 = I_{0(Ge)} e^{\frac{0.1435}{26\times10^{-3}}}$$

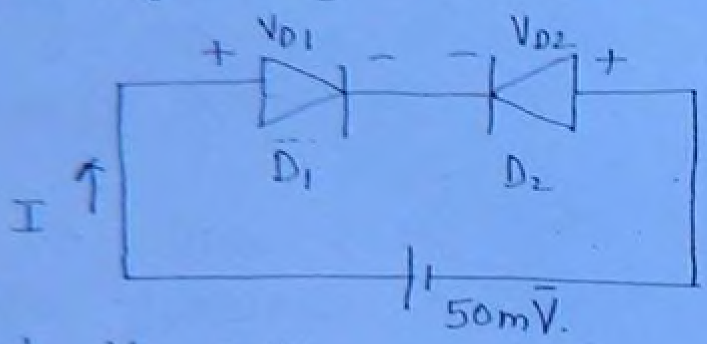
For Si

$$1 = I_{0(Si)} e^{\frac{0.718}{26\times10^{-3}\times2}}$$

$$\frac{I_0(Ge)}{I_0(Si)} = 3977$$ Ans.

(only for IES)

Ques The circuit given below consist of two identical diodes each value having a utility factor of unity Assume thermal Voltage 25 mV



Find V_{D1} & V_{D2}.

Sol^n In the given circuit D_1 is FB and non-conductive and D_2 is RB & non conducting.

→ The forward current of D_1 will be flowing as reverse current in D_2.

For D_1

$$I = I_F = I_0\left[e^{+\frac{V_{d1}}{\eta V_T}} - 1\right] \rightarrow (1)$$

For D_2

$$I = I_0 = -I_0\left[e^{-\frac{V_{d2}}{\eta V_T}} - 1\right] \rightarrow (2)$$

equating (1) & (2)

$$I_0\left[e^{\frac{V_{d1}}{\eta V_T}} - 1\right] = -I_0\left[e^{-\frac{V_{d2}}{\eta V_T}} - 1\right]$$

$$e^{\frac{V_{d1}}{\eta V_T}} - 1 = -e^{-\frac{V_{d2}}{\eta V_T}} + 1$$

$$e^{\frac{V_{d1}}{\eta V_T}} + e^{-\frac{V_{d2}}{\eta V_T}} = 2 \Rightarrow e^{\frac{V_{d1}}{\eta V_T}} - e^{-\frac{(50-V_{D1})}{\eta V_T}} = 2$$

$\{\because V_{D1} + V_{D2} = 50 \Rightarrow V_{D2} = 50 - V_{D1}\}$ $\Rightarrow e^{\frac{V_{d1}}{\eta V_T}}[1 + e^{-2}] = 2$

$\Rightarrow V_{D1} = \eta V_T \log_e \frac{2}{1+e^{-2}} \Rightarrow$ $\boxed{V_{D1} = 14.15\,mV}$ y/1

→ In above circuit none of diode will be conducting but one diode is FB and non-conducting & other diode is RB and non conducting

→ This ckt is used in power supply as overload protection ckt or short ckt protection ckt

(1) (Conventional page no 12)

soln

$$e^{\frac{V_{D1}}{\eta V_T}} + e^{-\frac{V_{D2}}{\eta V_T}} = 2.$$

$$e^{\frac{V_{D1}}{\eta V_T}} + e^{-\frac{(5-V_{D1})}{\eta V_T}} = 2.$$

$$e^{\frac{V_{D1}}{\eta V_T}} + e^{-\frac{(5-V_{D1})}{\eta V_T}} = 2$$

$$e^{\frac{V_{D1}}{\eta V_T}} + e^{-50} \cdot e^{\frac{V_{D1}}{\eta V_T}} = 2$$

$$e^{\frac{V_{D1}}{\eta V_T}} (1 + e^{-50}) = 2$$

$$V_{D1} = \eta V_T \log_e \frac{2}{1+e^{-50}}$$

$$V_{D1} = 2 \times 25 \times 10^{-3} \log_e \frac{2}{1+e^{-50}}$$

$$V_{D1} = 34.325$$

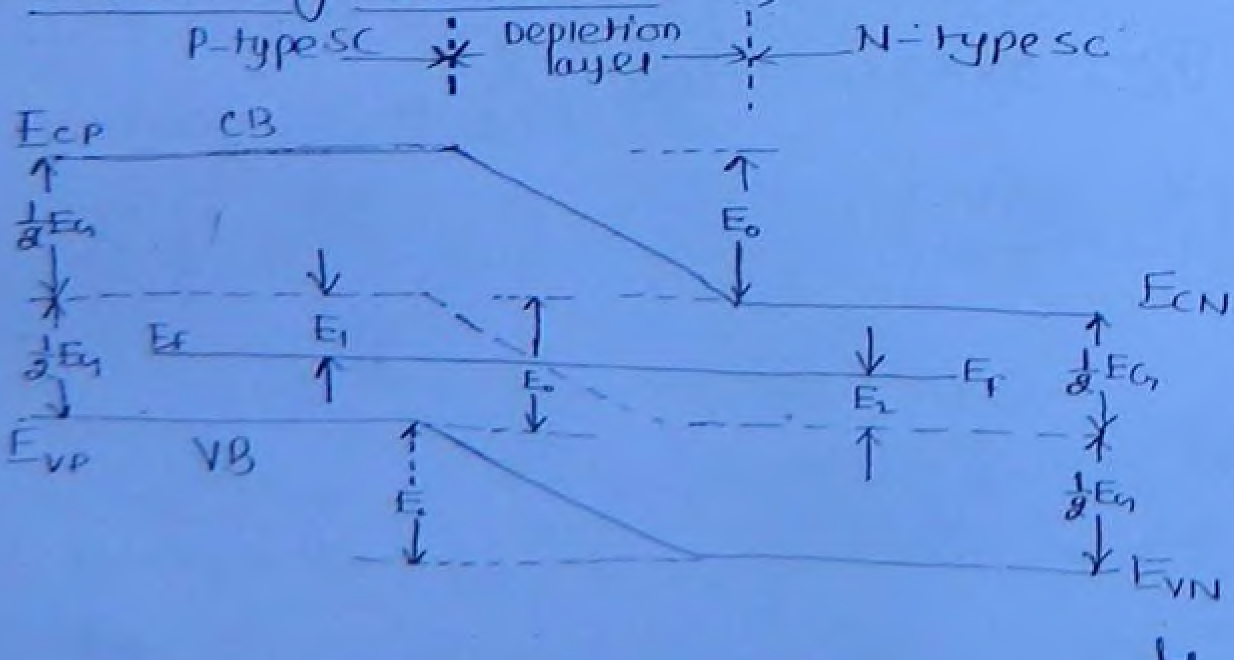
Draw the energy band diagram of OC p-n junction diode and derive an equation for contact potential of diode.

→ In p-type SC at room temperature, fermi level will be exiting just above the acceptor energy level.

→ In N-type SC at room temperature the fermi level will be existing just below the donor energy level.

→ When P-N-junction is created the energy band diagram of p and N-region will be adjusted so that the fermi level will maintain a straight line force.

→ The energy band diagram of OC PN junction diode is given below ⟹



→ In the above diagram E_0 is the potential energy of the e^- at the junction expressed in eV.

→ In the diagram

$$\Rightarrow \boxed{E_0 = E_{CP} - E_{CN} = E_{VP} - E_{VN} = E_1 + E_2} \rightarrow (1)$$

$$\Rightarrow \boxed{E_F - E_{VP} = \frac{1}{2} E_G - E_1} \rightarrow (2)$$

$$\Rightarrow \boxed{E_{CN} - E_F = \frac{1}{2} E_G - E_2} \rightarrow (3)$$

→ Adding eq (2) & (3)

$$\Rightarrow (E_F - E_{VP}) + (E_{CN} - E_F) = E_G - (E_1 + E_2)$$

from eq (1), $E_1 + E_2 = E_0$

$$\Rightarrow (E_F - E_{VP}) + (E_{CN} - E_F) = E_G - E_0$$

$$\Rightarrow \boxed{E_0 = E_G - (E_F - E_{VP}) - (E_{CN} - E_F)} \quad \text{---} (4)$$

from p-type SC

$$\Rightarrow E_F - E_{VP} = KT \cdot \log_e \frac{N_V}{N_A} \quad \text{---} (A)$$

From N-type SC

$$\Rightarrow E_{CN} - E_F = KT \log_e \frac{N_C}{N_D} \quad \text{---} (B)$$

from the derivation of n_i :

$$n_i^2 = N_c N_v e^{-E_G/KT}$$

$$\Rightarrow \boxed{E_G = KT \log_e \frac{N_c N_v}{n_i^2}} \quad --- \quad (C)$$

⇒ Substituting (A), (B), & (C) in eq (4)

$$E_0 = KT \log_e \frac{N_c N_v}{n_i^2} - KT \log_e \frac{N_v}{N_A} - KT \log_e \frac{N_c}{N_D}$$

$$E_0 = KT \log_e \left[\frac{N_c N_v}{n_i^2} \times \frac{N_A}{N_v} \times \frac{N_D}{N_c} \right].$$

$$\star \Rightarrow \boxed{E_0 = KT \log_e \frac{N_A N_D}{n_i^2}} \; eV.$$

It is the equation for the potential energy of e^- at the junction.

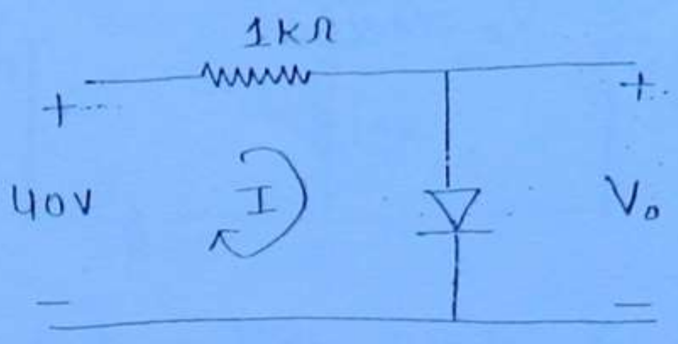
The contact potential of the diode is denoted by V_0 ; & it is numerically equal to potential energy of e^- expressed in V.

$$\Rightarrow \boxed{V_0 = V_T \log_e \frac{N_A N_D}{n_i^2}} \; Volt$$

Simple Diode Circuits :→

① Ideal Diodes :→

find I and V_o

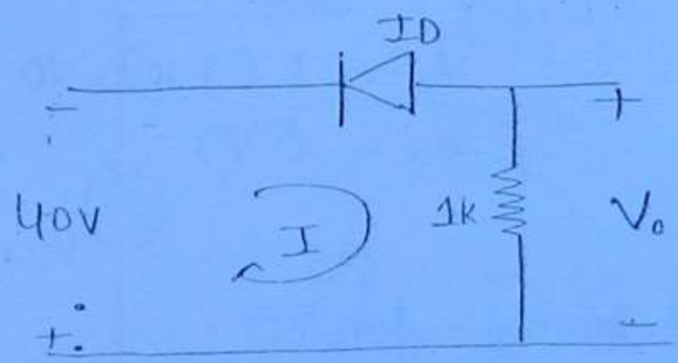


ID is FB & SC

$V_o = 0$

$I = \frac{40}{1K} = 40mA.$

find I & V_o



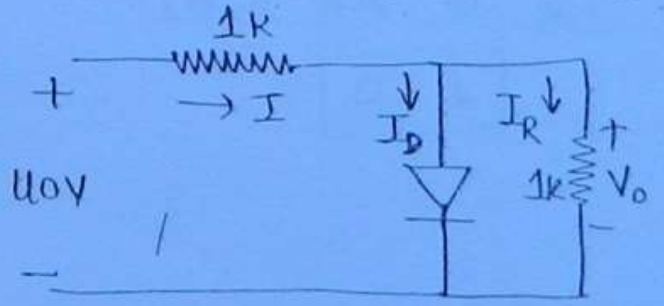
ID is FB & SC

$V_o = -40V$

$I = \frac{V_o}{1K} = \frac{-40}{1K}$

$I = -40mA.$

find V_o, I I_R & I_D

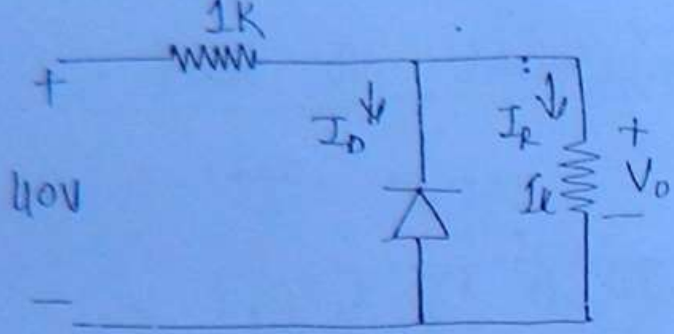


ID is FB & SC.

$V_o = 0$

$I_R = 0$

$I = I_D = \frac{40}{1K} = 40mA$



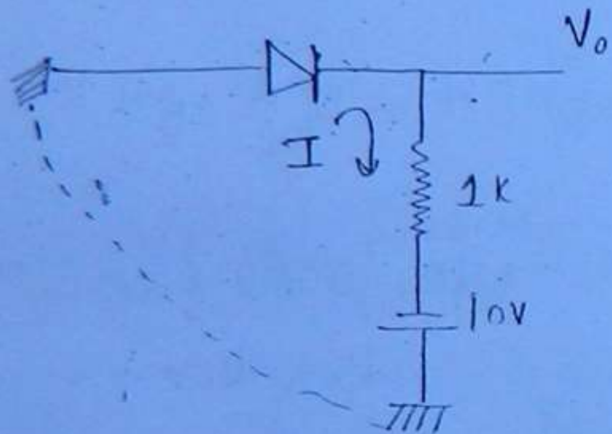
ID is RB & OC.

$I_D = 0$

$I_R = I = \frac{40V}{2k} = 20mA$

$V_o = 20V.$

find I & V_o



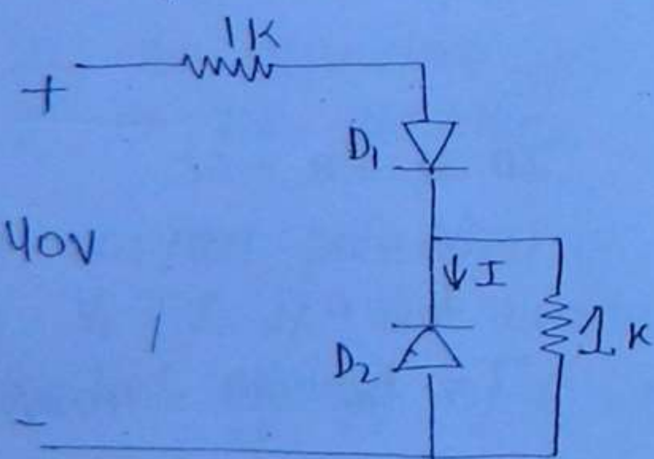
ID is FB & SC

$I = \frac{10V}{1K} = 10mA$

$V_o = I(1K) - 10$

$V_o = 0V$

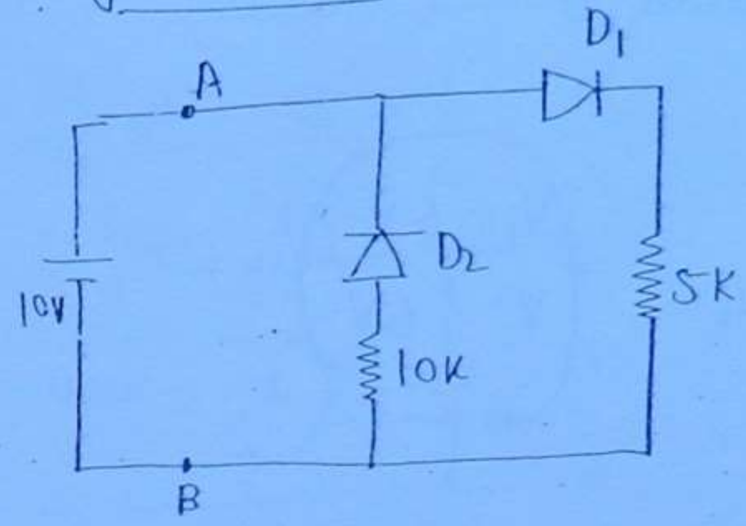
Assuming D_1 & D_2 are ideal diodes find I.



D_2 is RB & OC

$I = 0$

find Z_{AB}



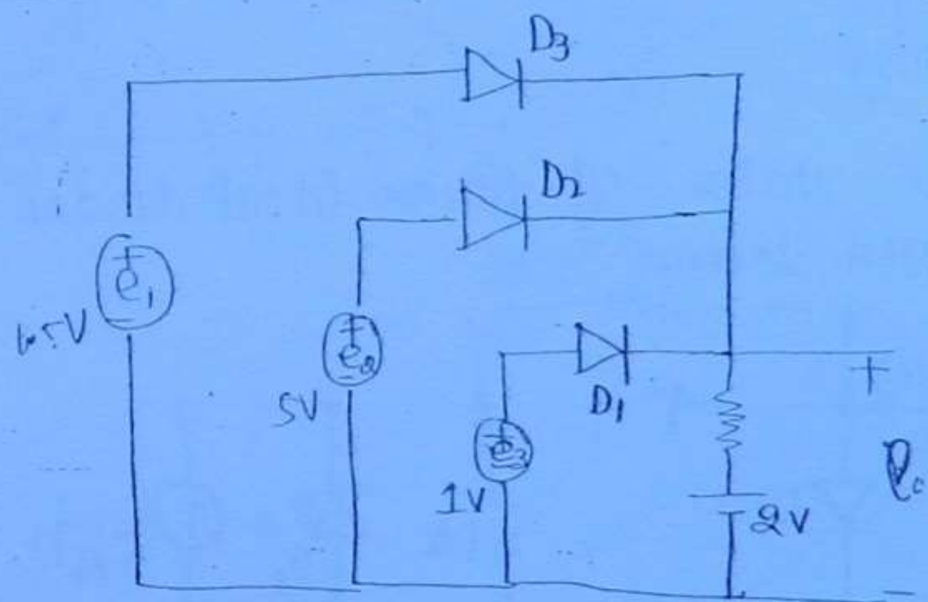
A is +ve w.r.t. B

D_1 is FB & SC

D_2 is RB & OC

$\Rightarrow$ $\boxed{Z_{AB} = 5\,k\Omega}$

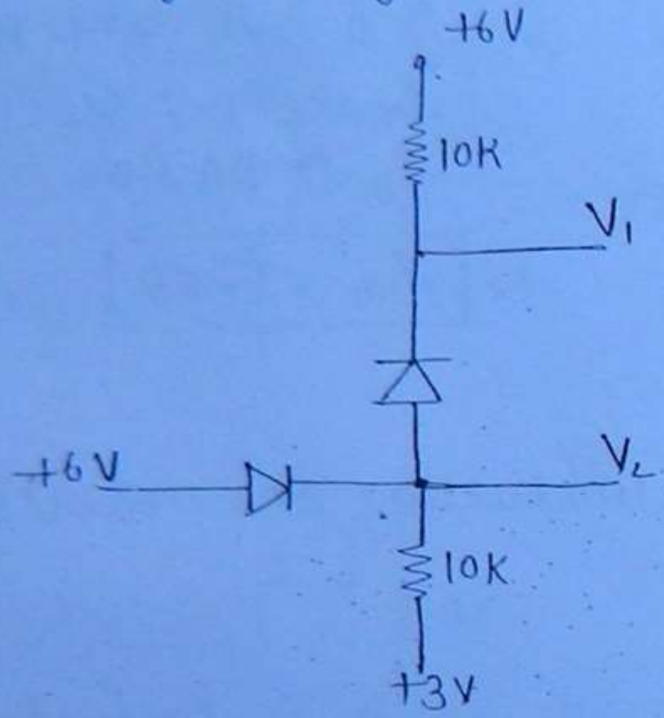
Ques: find which Diode is conducting in circuit and also find e_o.



D_2 is conducting

$\Rightarrow$ $\boxed{e_o = 5V}$

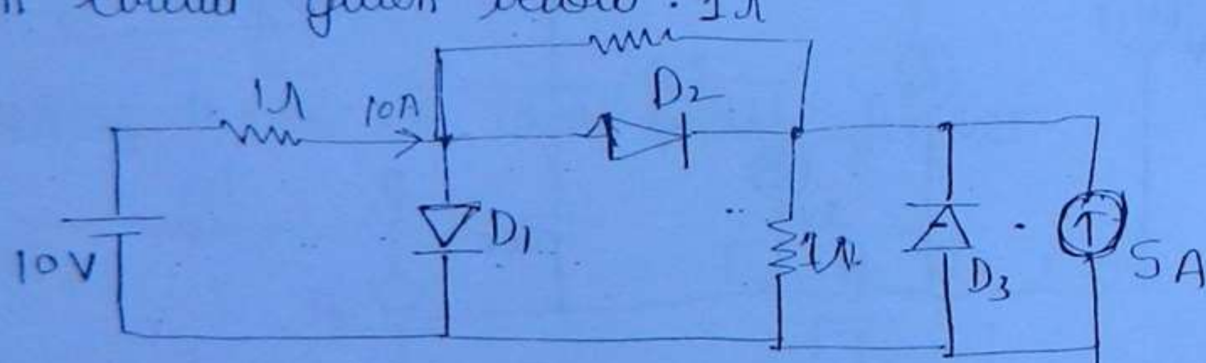
Prob : The voltages at V_1 & V_2 for the circuit arrangement given below is



$V_1 = 6\,V$

$V_2 = 6\,V$

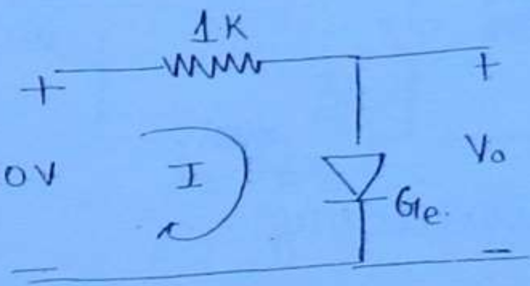
Prob What are the states of three ideal diodes in circuit given below.



D_1 ON FB D_2 OFF RB D_3 OFF RB   Ans.

(ii) Practical Diode Circuits :→

Find I & V_o



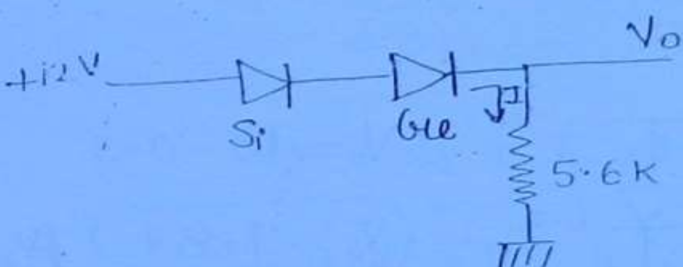
Ge D is FB & replaced by

$$V_o = V_{\gamma Ge} = 0.2V.$$

$$I = \frac{40 - V_{\gamma Ge}}{1K}$$

$$I = 39.8\ mA.$$

Find I & V_o



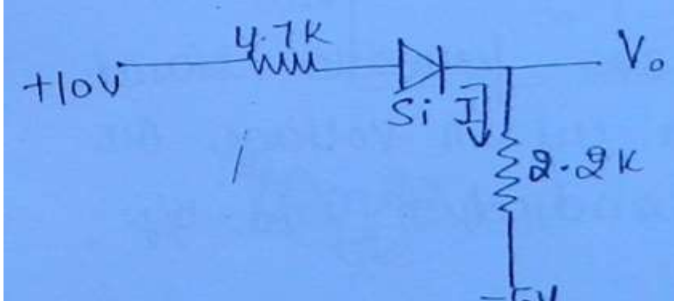
$$V_o = 12 - V_{\gamma Si} - V_{\gamma Ge}$$

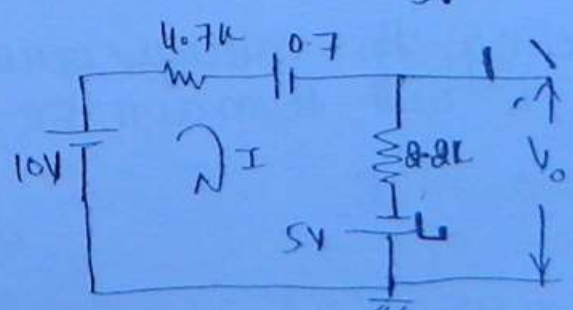
$$= 12 - 0.7 - 0.2$$

$$= 11.1\ V$$

$$I = \frac{V_o}{5.6K} = 1.98\ mA$$

Find I & V_o





$$I = \frac{5 + 10 - 0.7}{6.9}$$

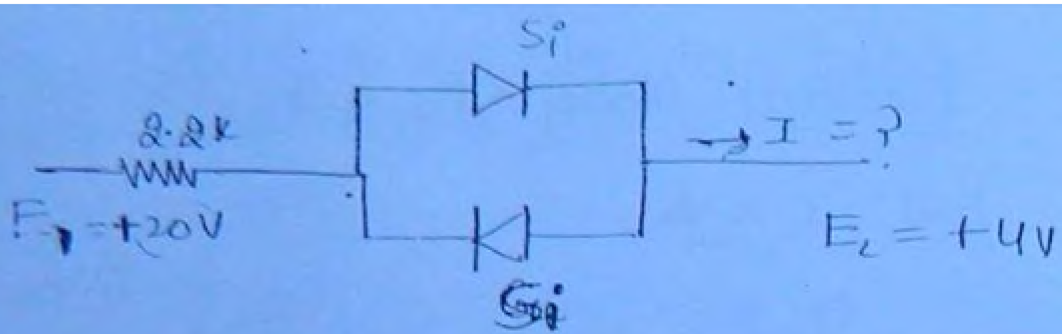
$$I = 2.07\ mA$$

$$V_o = I(2.2K) - 5$$

$$= 4.55 - 5$$

$$= -0.45V.$$

Prob



Soln

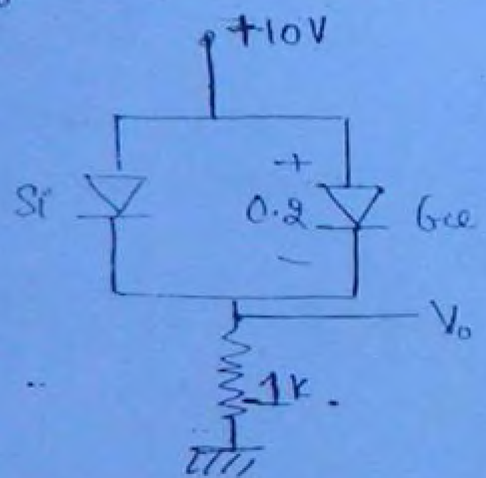
$E_1 > E_2$

UD is FB & conducting

$$I = \frac{20 - 4 - 0.7}{2.2K} = 6.95\,mA$$ Ans.

Prob find V_o

{ $V_{\gamma Si} > V_{\gamma Ge}$
0.7 > 0.2
so Ge D i'r conducting }



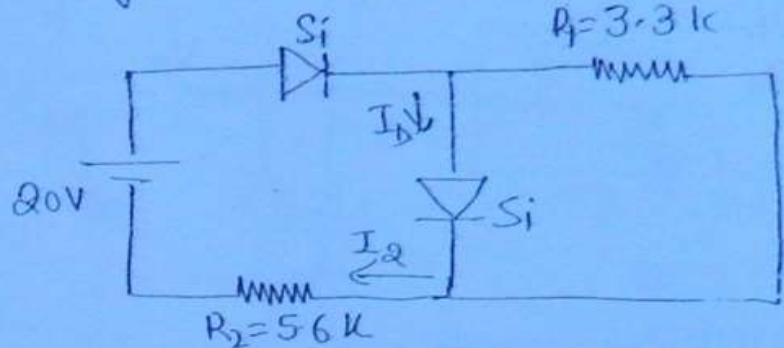
$V_o = 10 - 0.2$

$V_o = 9.8V$ Ans.

→ Both Ge & Si Diode are forward biased but because of smaller cut in voltage Ge diode will enter into conduction and o/p voltage is 9.8V Ans.

→ When Ge diode is conducting, the voltage across Si diode is 0.2 V therefore it will remain FB & non-conducting.

Prob find I_D



$$I_2 = \frac{20 - 0.7 - 0.7}{5.6}$$

$$I_2 = \frac{20 - 1.4}{5.6}$$

$$I_2 = \frac{18.6}{5.6}$$

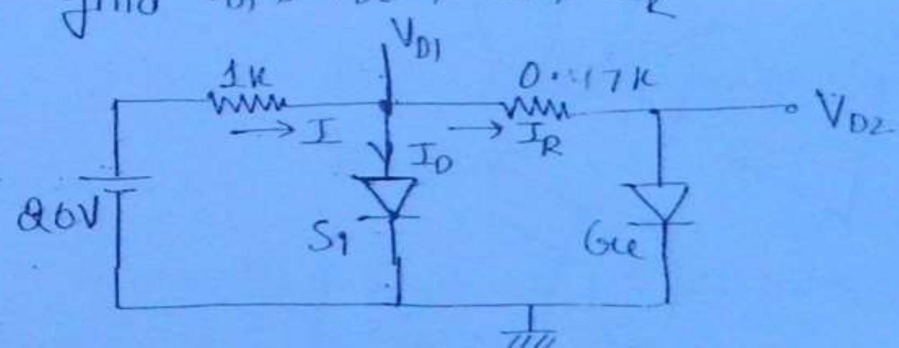
$$\boxed{I_2 = 3.321\ mA}$$ Ans

$$V_{R1} = V_{\gamma Si} = 0.7\ V.$$

$$I_1 = \frac{0.7V}{3.3k} = 0.212\ mA$$

$$I_2 = I_D + I_1 \Rightarrow \boxed{I_D = 3.109\ mA}$$

Prob find V_{D1} & V_{D2} & I & I_R



$$V_{D1} = V_{\gamma Si} = 0.7\ V.$$

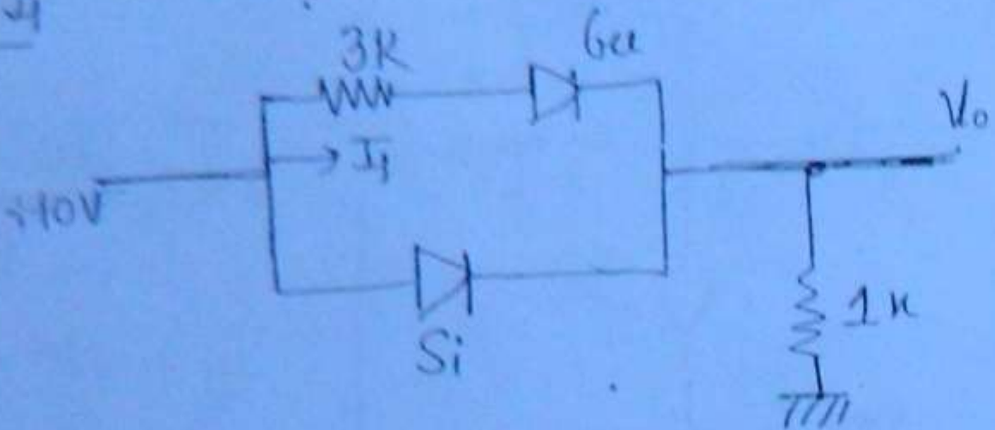
$$V_{D2} = V_{\gamma Si} = 0.2V.$$

$$I = \frac{20 - 0.7}{10k} = \frac{19.3}{10k} = 19.3\ mA$$

$$I_R = \frac{0.7 - 0.2}{0.47} = \frac{0.5}{0.47} = 1.06\ mA$$

$$I_D = 19.3 - 1.06 = 18.24\ mA$$

Find V_0 & I_1



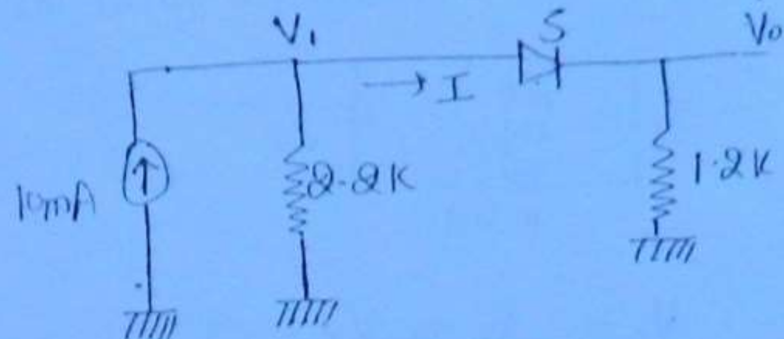
Both Ge & Si diode will be conducting

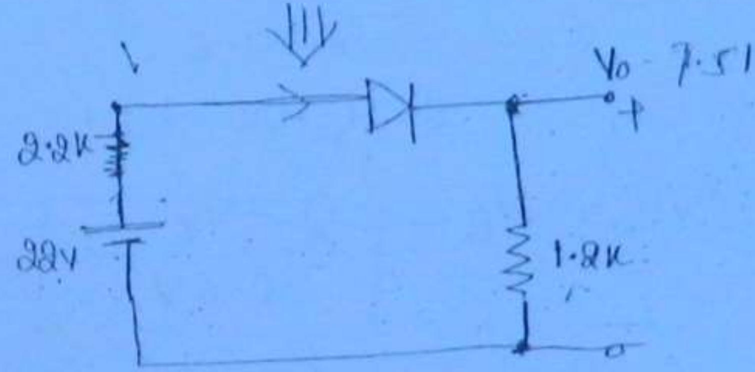
$$V_0 = 10 - V_{\gamma si}$$
$$= 10 - 0.7$$
$$= 9.3V$$

$$I_1 = \frac{0.5V}{3k} = 0.1667\ mA$$

END OF DAY

Find I, V, and V_0.





$$I = \frac{22 - 0.7}{2.2 + 1.2} = 6.26\,mA$$

$$V_1 = 22 - I(R)$$

$$= 22 - 6.26\,mA\,(2.2\,k\Omega)$$

$$= 8.21\,V$$

$$V_0 = V_1 - V_{\gamma si} = 8.21 - 0.7 = 7.51\,V.$$

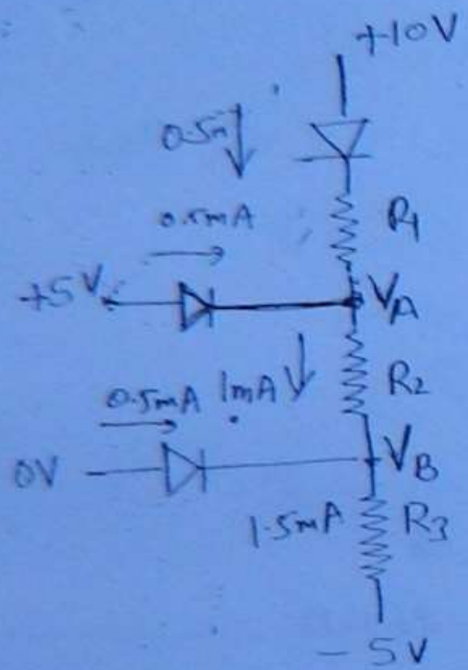
or

$$V_0 = IR$$

$$= 6.26\,mA\,(1.2\,k)$$

$$= 7.51\,V$$

The cutin voltage for each diode is 0.6 V and each diode current is 0.5mA. find the values of R_1, R_2 & R_3.



$$V_A = 5 - V_\gamma = 5 - 0.6 = 4.4V$$

$$V_B = 0 - V_\gamma = -0.6V$$

$$R_1 = \frac{10 - V_\gamma - V_A}{0.5}$$

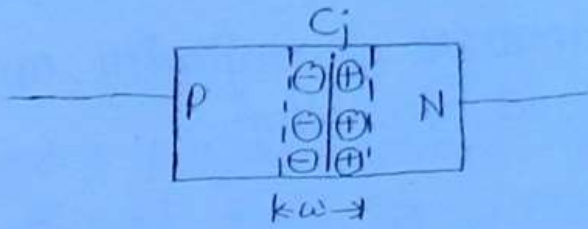
$$R_1 = \frac{10 - 0.6 - 4.4}{0.5}$$

$$\boxed{R_1 = 10K\Omega}$$

$$R_2 = \frac{V_A - V_B}{1mA} = \frac{4.4 - (-0.6)}{1mA} = 5K\Omega$$

$$R_3 = \frac{V_B + 5}{1.5} = \frac{-0.6 + 5}{1.5} = \frac{4.4}{1.5} = 2.97K\Omega$$

Junction Capacitance (C_j)



$$C_j = \frac{\epsilon_0 \epsilon_r A}{\omega}$$

- let $\epsilon_0 \epsilon_r = \varepsilon$

$$\Rightarrow \boxed{C_j = \frac{\epsilon A}{\omega}}$$

The depletion layer in a p-n junction diode will be working as a parallel plate capacitor.

$$\Rightarrow \boxed{C_j \propto A}$$

$$\Rightarrow \boxed{C_j \propto \frac{1}{\omega}}$$

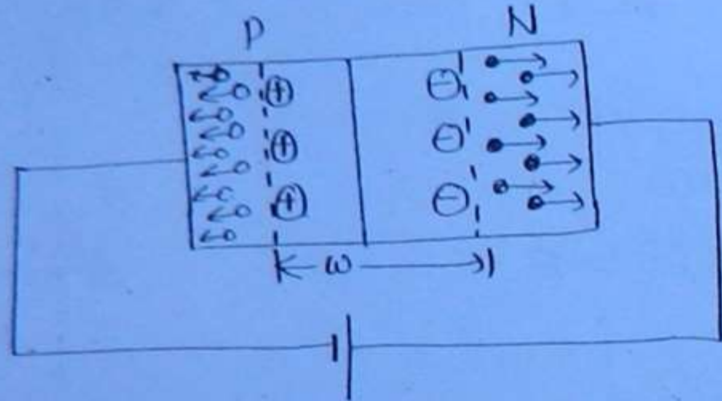
$C_j \rightarrow$ pF i.e. 10^{-12} F

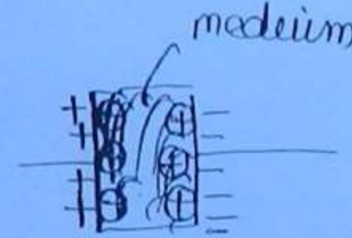
⇒ When diode is unbiased or OC, both C_T and C_D will be appearing in the diode. and then biasing is provided one of the capacitance will be dominating.

⇒ $C_T \rightarrow$ Transition capacitance also called Depletion layer capacitance or space charge capacitance

→ C_T is the junction capacitance dominated in a reverse biased diode.

→ C_T is due to the storage of majority carriers across the reverse biased junction.





$$C_T = C_j = \frac{\epsilon A}{\omega}$$

⇒ $C_T \propto A$

$C_T \propto \frac{1}{\omega}$

⇒ $C_T \propto \sqrt{\text{Doping}}$ since $\omega \propto \frac{1}{\sqrt{\text{Doping}}}$.

⟹ $C_T \propto \frac{1}{\sqrt{V_j}}$ since $\omega \propto \sqrt{V_j}$

$C_T \propto \frac{1}{\sqrt{V_{bi} + V_{RB}}}$ since $\omega \propto \sqrt{V_{bi} + V_{RB}}$

neglecting V_{bi}

⟹ $C_T \propto \frac{1}{\sqrt{\text{RB voltage}}}$

Typical Values

C_T = 3pF for BJT → Better performance.
5pf for Diode

→ for better performance of diode or BJT, C_T value must be as small as possible.

→ The property of C_T is used in designing of the varactor diode.

→ In a Reverse biased diode the transition capacitance C_T

$$C_T \propto V^{-1/2}$$

$$C_T \propto V^{-n}$$

↑ Applied reverse voltage and n is a constant is given by

- Imp.

$n = \frac{1}{2}$ for step graded diode.

$n = \frac{1}{3}$ for linear graded diode.

$n = \frac{1}{2.5}$ for diffused p-N junction diode

n = grading coefficient and its value depends on concentration gradient.

→ C_T will appear in device both during the low frequency and high frequency operation.

C_D (Diffusion Capacitance)

→ Also called storage capacitance.

→ C_D is the junction capacitance dominating in forward biased diode.

→ C_D is due to storage of minority carriers across forward biased diode.

→ It is storing the minority carriers across the junction and therefore called <u>storage capacitance</u>.

$$C_D = C_j = \frac{\epsilon A}{\omega}$$

$$\Rightarrow \boxed{C_D \propto A \qquad C_D \propto \frac{1}{\omega}}$$

$$\Rightarrow \boxed{C_D \propto \sqrt{Doping}} \quad \text{since} \quad \omega \propto \frac{1}{\sqrt{Doping}}$$

$$\boxed{C_D \propto \sqrt{FB}} \quad \text{since} \quad \omega \propto \frac{1}{\sqrt{F \cdot Biased}}$$

→ High frequency operation of a diode or BJT is limited by presence of C_D.

→ $\boxed{C_D = \tau . g}$ $\qquad g = \frac{1}{r}$

$$\boxed{C_D = \frac{\tau}{r}} \Rightarrow \boxed{C_D = \frac{\tau I_f}{\eta V_T}} \qquad \boxed{C_D \propto I_f}$$

→ Diffusion capacitance linearly increases with forward current.

but $I_f \approx I_o e^{V_d/\eta V_T}$

$$\Rightarrow \boxed{C_D = \frac{\tau I_o e^{\frac{V_d}{\eta V_T}}}{\eta V_T}}$$

→ Diffusion capacitance exponentially increases with forward voltage across the diode.

Carrier lifetime (τ) :→

or mean lifetime of minority carriers.
or average lifetime (μ sec to n sec)

$$\Rightarrow \boxed{\tau = \frac{C_D}{g} = C_D \cdot r = \frac{C_D \eta V_T}{I_f} \text{ sec}}$$

→ Derive an equation for transition capacitance C_T

C_T is the junction capacitance in a RB diode

$$C_T \Rightarrow C_j = \frac{\epsilon A}{\omega} \text{ farad.}$$

$$\omega = \sqrt{\frac{2\epsilon}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_o + V_{RB})}$$

$$\Rightarrow C_j = \frac{\epsilon A}{\sqrt{\frac{2\epsilon}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_o + V_{RB})}}$$

⟹ Dividing numerator and Denominator ϵ

$$C_j = \frac{A}{\sqrt{\frac{2}{q\epsilon}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(V_0+V_{RB})}}$$

$$C_j = \frac{A}{\sqrt{\frac{2}{q\epsilon}\left(\frac{N_A+N_D}{N_A N_D}\right)V_0\left(1+\frac{V_{RB}}{V_0}\right)}}$$

$$C_j = \frac{A\sqrt{\frac{q\epsilon}{2V_0}\left(\frac{N_A N_D}{N_A+N_D}\right)}}{\sqrt{1+\frac{V_{RB}}{V_0}}}$$

if $V_{RB}=0$

$C_j = C_{j0}$ = junction capacitance of diode when $V_{RB}=0$.

$$\Rightarrow \boxed{C_{j0} = A\sqrt{\frac{q\epsilon}{2V_0}\left(\frac{N_A N_D}{N_A+N_D}\right)}} \text{ Farad}$$

C_{j0} can be expressed per cross sectional area

$$\Rightarrow \boxed{C_{j0} = \sqrt{\frac{q\epsilon}{2V_0}\left(\frac{N_A N_D}{N_A+N_D}\right)}} \text{ F/m}^2$$

Imp $\boxed{C_j = \frac{C_{j0}}{\left(1+\frac{V_{RB}}{V_0}\right)^{1/2}}}$ Farad

($C_j \to C_T$)

→ The transition capacitance can be expressed in generalised form :→

Imp ⟹ $$C_j = \frac{C_{j0}}{\left(1 + \frac{V_{RB}}{V_0}\right)^m}$$

$m \Rightarrow$ grading coefficient.

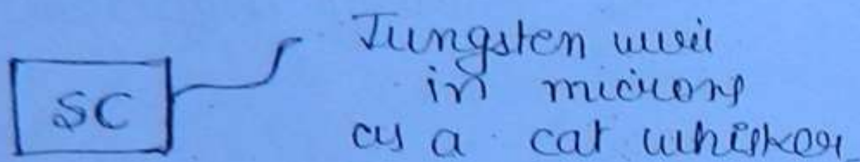
Point Contact Diode

→ Earliest diode or first diode (100 years old)

→ metal semiconductor junction diode.

→ The least value of junction capacitance is obtained with point contact diode.

→



VARACTER DIODE :→

→ It is a linear graded diode

→ This is working on the principle of transition capacitance.

→ Always operated under reverse biased

→ $C_T \propto V^{-n}$, where $n = \frac{1}{3}$ for VD.

$$\Rightarrow C_T \propto \frac{1}{\sqrt[3]{\text{RB voltage}}}$$

$$\Rightarrow C_T \propto \frac{1}{\sqrt[3]{V_{bi} + V_{RB}}}$$

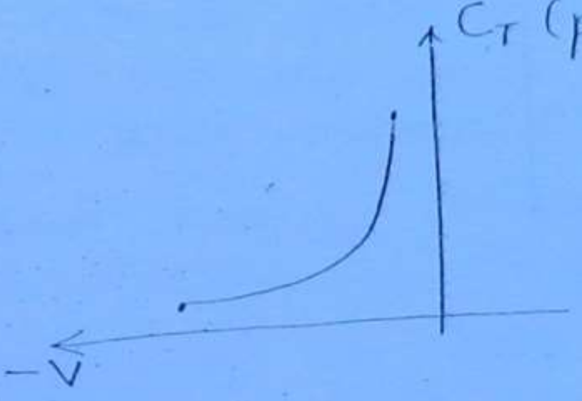
⇒ As VD is more RB the C_T ↓

→ Popularly used material GaAs.

→ Low Noise Device.

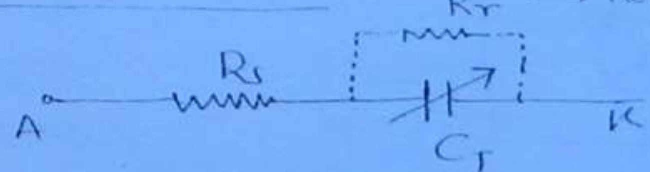
→ By varying RB voltage we get a small variation in C_T (in pf).

→ characteristic curve of VD.



→ Symbol

→ Equivalent circuit.



R_s → ohmic resistance or contact resistance or Bulk resistance. (<10 Ω).

→ Also called VARI-CAP (variable capacitance Diode) or VOLTA-CAP (voltage variable capacitance) or epi-cap.

→ (1) Varactor Diode used as Para-Amp^r.

→ **Applications** :→ (2) For Direct generation FM frequency by using varactor diode modulator circuit.

(3) For self balancing AC bridges. (4) for electronic tuning of receiver (5) Fine tuning of receiver (5) for tuning of LC resonant ckt.

(6)

LED (Light Emitting Diode)

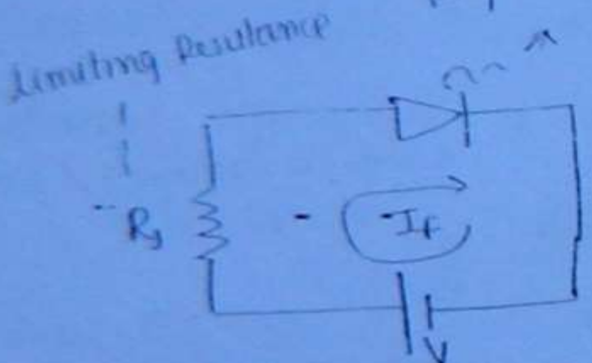
→ Based on principle electro-luminescence..

→ DBG-SC GaAs { IBG-SC GaP } → under special doping condn

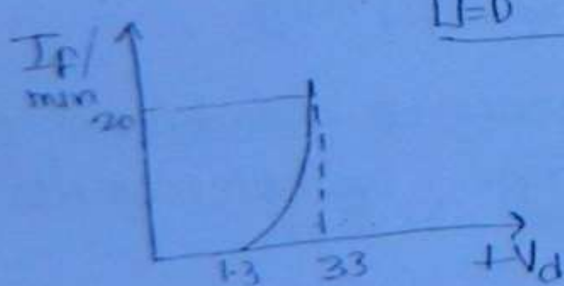
$$\lambda = \frac{1.24}{E_g} \mu m$$

$$\lambda = \frac{c}{f}$$

→ 



LED characteristics

→ 

→ LED will emit the light when properly biased

→ the best electroluminescent device is LED

→ Generally fabricated with DBG-SC

→ Popularly used material is GaAs

→ LED can be fabricated with DBG-SC materials and also with some of the IBG-SC material under controlled doping.

→ In LED light is emitted due to a large no. of recombination at the junction.

→ LED can emit the light either in the visible spectrum or invisible spectrum of light.

→ In the invisible spectrum LED emits IR light

→ IR LED is used as remote control trans...

→ In the visible spectrum of light LED can emit any one of the following colour such that

RED	YELLOW
GREEN	WHITE
ORANGE	AMBER.

→ The colour of light given by LED depends on
(1) The wavelength of radiated light.
(2) The frequency of radiated light
(3) The type of dopant
(4) The concn of dopant

→ LED fabricated with GaAs will emit IR light

→ LED materials are

GaAs → IR light
GaAsP → O
└→ Y
GaP → Green or Red

→ LED is always operated under forward biased

→ with 20mA of forward current LED gives out the maximum intensity of light.

→ If LED is heated up (temp increasing) then its efficiency decreases.

→ When Reverse biased LED will be working as a normal Diode and therefore it will not emit any light

→ Power dissipation in mW.

→ Response time in μsec.

→ Operating Life 1,00,000 + hrs.

→ Cut in voltage 1·3 to 1·5 V. depend on dopant.

→ LED is faster than LCD. (because of smaller response time)

- When compared to LCD the Disadvantages of LED is higher power dissipation applications.

Applications

(1) As a Remote control transmitter

(2) In designing of opto-coupler.

(3) As a display device.

Prob A GaAs LED is operating at room temp. find its wavelength of radiation

Soln

$$\lambda = \frac{1.24}{E_G}\ \mu m.$$

For GaAs, $E_{G300} = 1.47\ eV$.

$$\lambda = \frac{1.24}{1.47}\ \mu m = 0.843\ \mu m.$$

- Since $\lambda > 0.76\ \mu m$, GaAs LED will emits IR ligt

Prob A green colour LED emits light with a wavelength 5490 Å unit find the energy gap of material in eV.

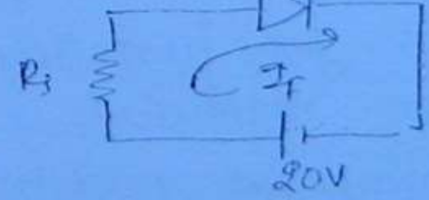
Soln

$$\lambda = \frac{1.24}{E_G}$$

$$5490 \times 10^{-10} \times 10^{6}\ \mu m = \frac{1.24}{E_G}$$

$$E_G = \frac{1.24}{5490 \times 10^{-4}} = 2.26\ eV.$$

Prob find the value of limiting resistance require for the LED circuit given below.

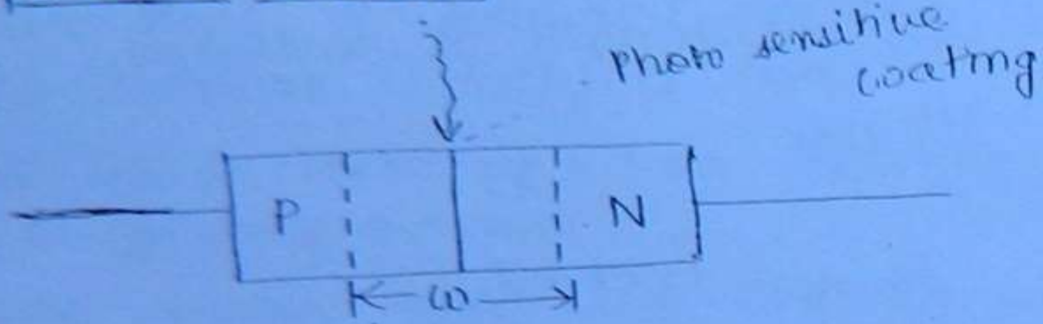


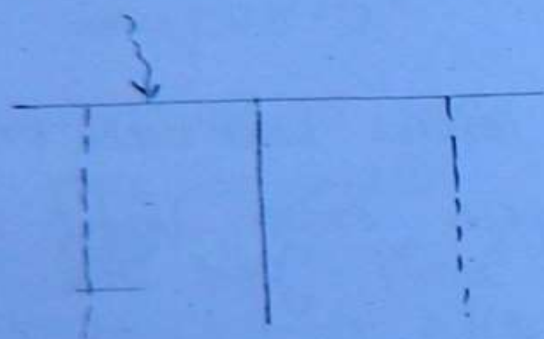
Soln let $I_F = 20mV$, $V_d = 3.3V$

$$20 = I_F R_s + V_d$$

$$\boxed{R_s = 835\ \Omega}$$ As

PHOTO-DIODE →



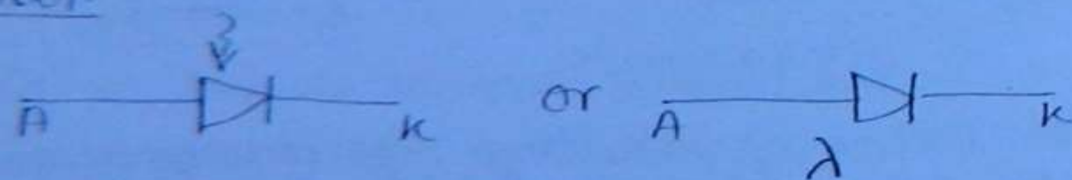


⇒ It will not conduct

Photosensitive material → (CdS, Se, ZnS, PbS.)

$$\omega \propto \frac{1}{\sqrt{\text{Doping}}}$$

Symbol



→ Photosensitive Device.

→ Basically a P-N junction for junction is coated with photosensitive material.

→ In a photodiode photosensitive coating is provided only at the junction.

→ In a PD if light falls slightly away from the junction then photodiode will not respond to light.

→ <u>Principle</u> → Photoconductive effect

→ Photosensitive materials are CdS, Se, ZnS, PbS.

→ PD has a larger depletion layer width and this is obtained by reducing the dopant concentration of P-N regions.

→ PD has very high sensitivity and this is due to larger depletion layer width.

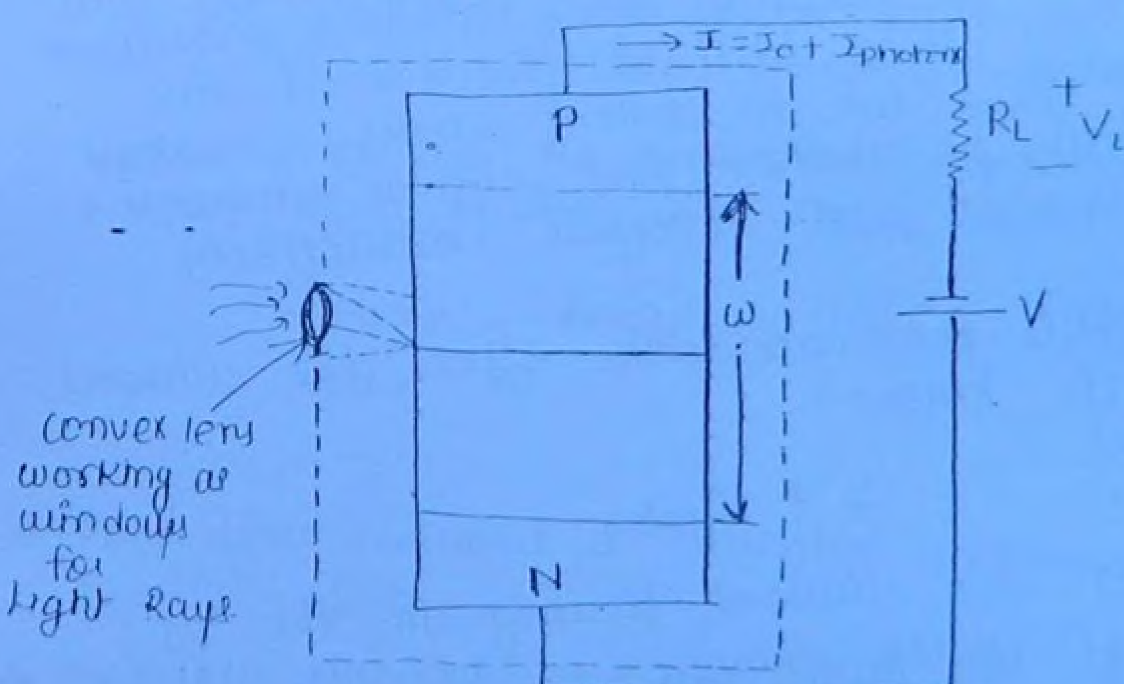
→ GePD will be responding to visible light

→ SiPD will be responding to Infrared light.

→ SiPD are used as a remote control sensor

→ PD is generally operated under RB.

→ For special application PD can be operated in OC cond^n or SC cond^n



→ When PD is operated under complete darkness i.e. no light is falling on the device.

PD will be working as a Normal Diode under RB.

$\Rightarrow$ $\boxed{I = I_0}$ → minority carrier current or Dark current. (I_{Dark})

$$\Rightarrow \left\{ \begin{array}{ll} I_{Dark} = \mu A & \text{for Ge PD} \\ \quad\quad\;\; nA & \text{for Si PD.} \end{array} \right\}$$

— At present photodiode is non-conducting i.e. "OFF STATE"

→ When light is focus at the window, maximum intensity of light will be focused at the junction and due to photon energy covalent bonds will be broken and charge carriers are increases and therefore conductivity increases.

→ Due to this photoconductive effect the current in PD is large

i.e, $I = I_c + I_{photon}$

→ I_{photon} is the current passing in the PD because of photon energy.

→ PD current has two current component

(1) Thermally generated current (I_0)

(2) Photon current (I_{photon})

→ In a photodiode photon current is added to the existing thermally generated current.

$I_{photon} > I_{Dark}$

I_{photon} ↓ mA

I_{Dark} ↳ μA Ge PD

nA Si PD.

$$\Rightarrow \boxed{I \approx I_{photon}}$$

→ Photodiode current flow from N to P

→ PD current is a Reverse current

→ PD current is a minority carrier current.

→ PD current is a diffusion current.

→ When light falls on the semiconductor minority carriers are created and these minority carriers will be moving from high concn to lower concn this due to the property called Diffusion

→ In a good PD the essential requirement is larger high photon to I_{Dark} ratio

$$\frac{I_{photon}}{I_{Dark}} = \text{large} = 10^3 : 1 \qquad 10^6 : 1$$

Ge PD — Si PD (Better performance)

→ Photodiode current is directly proportional to light flux.

→ Photodiode current increases with no. of photon falling at the junction.

→ The magnitude of reverse current in PD increases with intensity of light falling at the junction

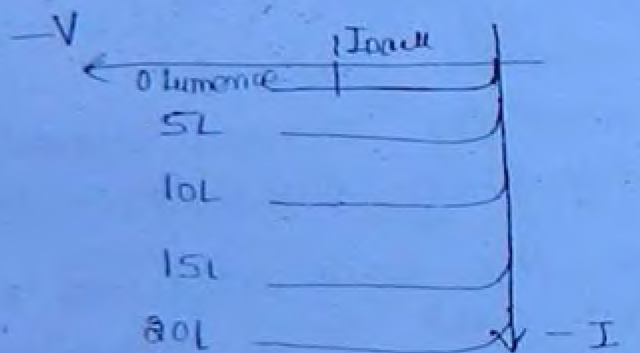
→ Equation for PD current

$$\Rightarrow \boxed{I = I_s + I_o\left[1 - e^{-V/\eta V_T}\right]}$$

I_s → SC current of PD.

$$\boxed{I \approx I_o\left[1 - e^{-V/\eta V_T}\right]}$$

→ PD characteristics will be plotted in III[rd] quadrant



L - lumen
unit for intensity of light.

→ PD current increases exponentially with light flux.

→ PD is basically a light operated switch
→ photodiode is a minority carrier injector.

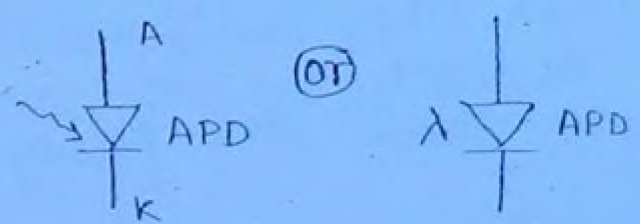
→ **Applications**

→ As a Remote control sensor.
→ In designing of opto coupler.
→ As a light operated switch.
→ To read audio track recorded on motion picture film.

→ When PD is FB & light is applied at the junction.
→ It will work as normal FB diode & current is due to majority carriers. The effect of light on majority carrier is zero & therefore forward current will remain const. i.e. current independent of light.

→ And also the PD can not be used as light operated switch.

AVALANCHE PHOTODIODE :→ GATE ONLY



→ Basically a photodiode along with avalanche effect always operated under RB.

→ Fabricated only with Si. comparatively can handle it more signal power.

→ Response time is very small (75ns).

→ APD is faster then PD. because of smaller response time.

→ ~~Measure~~ Major applications as a receiver in fibre optic communication system

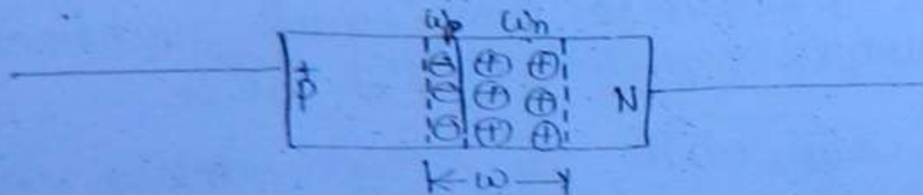
Types of JUNCTION :→

Normal junction → P & N region are equally doped

Abrupt junction → P & N region are different doping level. e.g. P^+N or PN^+

Step Graded Diode :→
or
Abrupt P-N junction diode.

→ It has abrupt junction ($P^{+}N$ or PN^{+} Diode)
→ Faster than Normal diode (due to higher doping concⁿ)
→ Depletion layer will be penetrating more into lightly doped region and lesser into highly doped region.



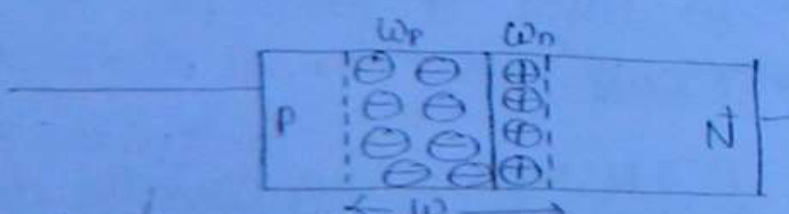
$N_A > N_D$

$W_N > W_P$

$W = W_N + W_P$

$\Rightarrow \boxed{W \simeq W_N}$

or



$N_D > N_A$

$W_P > W_n$

$W = W_N + W_P$

$\Rightarrow \boxed{W \simeq W_P}$

→ In a step graded diode, most of depletion layer will be exiting in the lightly doped region

→ When step graded diode is RB

(i) Considering P^+N Diode

The width of Depletion layer on the lightly doped region

$$\omega = \omega_n + \omega_p$$

$$\Rightarrow \boxed{\omega \simeq \omega_n}$$

$$\Rightarrow \boxed{\omega \simeq \sqrt{\frac{2\epsilon}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right) V_j}}$$

$N_A \rightarrow$ Highly doped so $\frac{1}{N_A}$ is neglected

☆ $$\Rightarrow \boxed{\omega = \sqrt{\frac{2\,\epsilon_0\,\epsilon_r\,V_j}{q\,N_D}}} \text{ metres.}$$

The junction voltage V_j

☆ $$\Rightarrow \boxed{V_j = \frac{q\,N_D\,\omega^2}{2\epsilon}} \text{ volts.}$$

(ii) Considering PN^+ diode.

$$\boxed{\omega \simeq \omega_p}$$

$$\omega \simeq \sqrt{\frac{2\epsilon}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right) V_j} \quad \left\{\frac{1}{N_D} \text{ is neglected}\right.$$

$$\Rightarrow \boxed{\omega \simeq \sqrt{\frac{2\epsilon V_j}{q N_A}}}$$

$$\Rightarrow \boxed{V_j = \frac{q\,N_A\,\omega^2}{2\epsilon}}$$

→ In a step graded diode the width of the depletion layers on the p- region and N- region can be directly obtained from charge equavality equation. given below :→

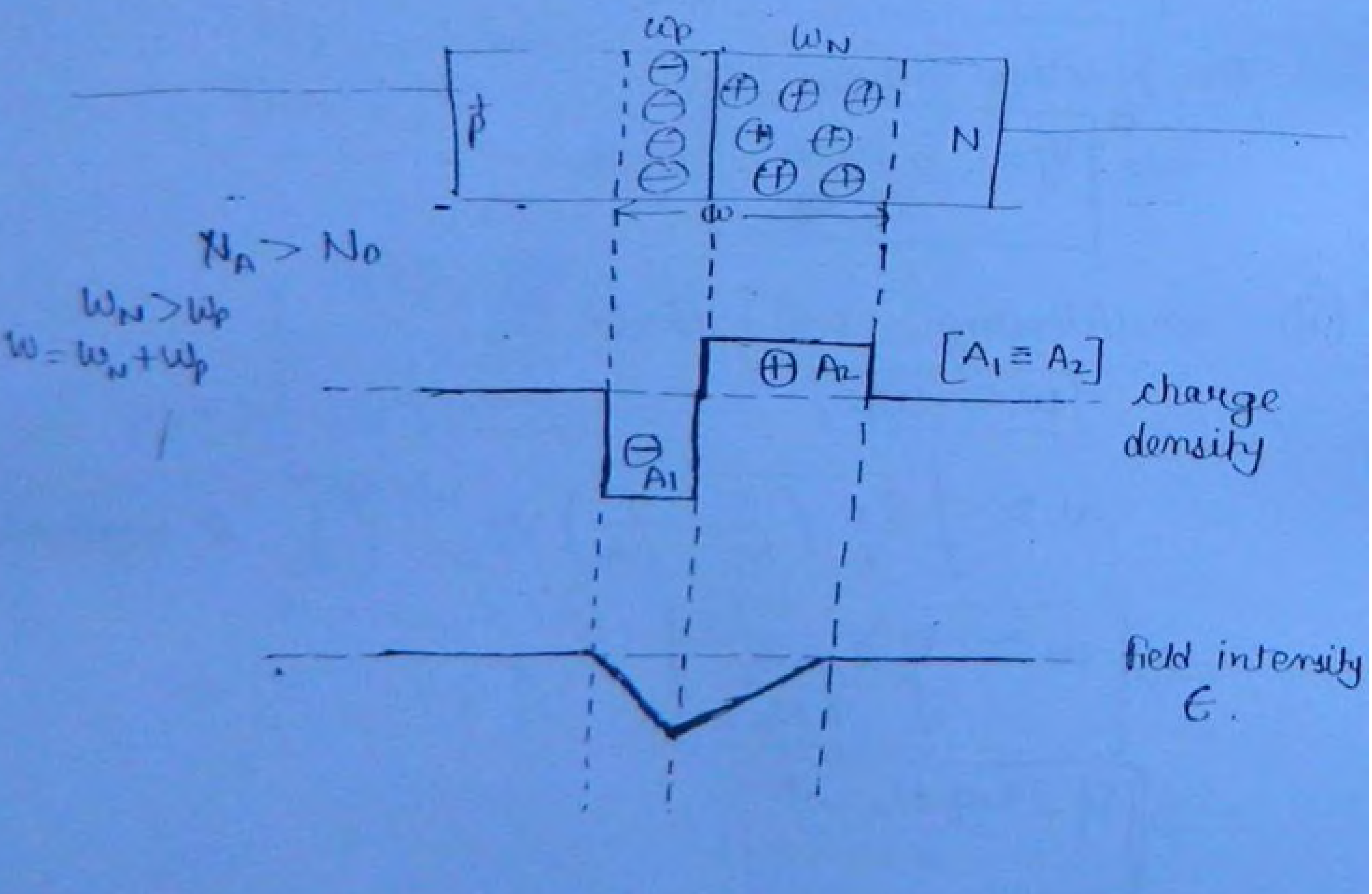
$$qA\,w_n N_D = qA\,w_p N_A$$

$$w_N N_D = w_P N_A$$

$$\Rightarrow \boxed{\frac{w_N}{w_D} = \frac{N_A}{N_D}}$$

→ The charge density curve and field intensity curve in a step graded diode is given below:

(1) Considering P^+N diode.



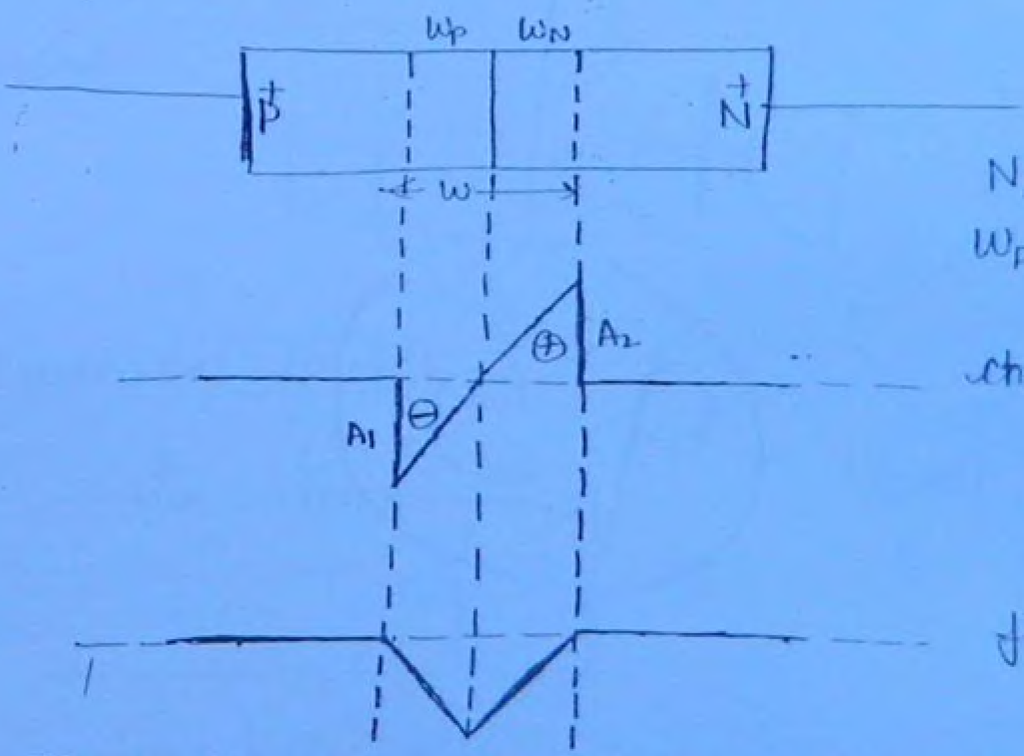
→ In step graded diode field intensity is maximum at the junction

→ In step graded diode field intensity is maximum at junction but it is not at the centre of depletion layer.

Linear Graded Diode :→ Conventional Ques^n

→ It is a P^+N^+ Diode with highly doped Diode with normal junction

→ The charge density diagram and field intensity curve for linear graded diode is given below:→



$N_A - N_D$

$W_P = W_N = \frac{W}{2}$

charge density

field Intensity ϵ

→ In a linear graded diode field intensity is maximum at junction (also max. at centre of depletion layer).

Tunnel Diode :→

or

Esaki Diode.

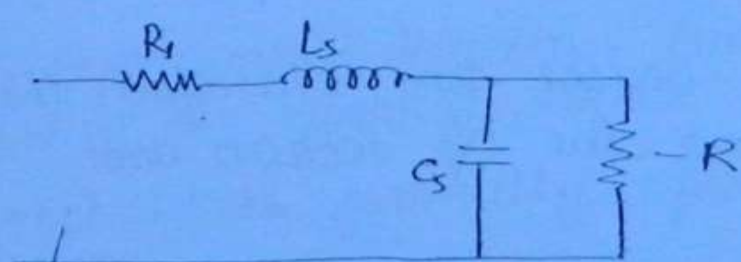
$P^+ N^+$ → Doped in $10^3 : 1$.

$$W \propto \frac{1}{\sqrt{Doping}}$$

Narrow Depletion $W = 100\,Å$ to $200\,Å$

Symol

Equivalent circuit



Typical value

$-R = -30\Omega$

→ Also called Esaki Diode

→ $P^+ N^+$ Diode with a normal junction

→ Doping concn $1 : 10^3$

Highly Doped Semiconductor Diode.

→ Popularily used material is GaAs

→ Low Noise Device

→ Narrow Depletion layer. (100 Å to 200 Å).

→ Fastest switch.

→ Switching time psec (10^{-12} sec).

→ Negative Resistance Device.

→ Tunnel Diode is more popular as a -ve resistance Device for but not as a fast switch.

→ Tunnel Diode exhibit the property of tunnelling effect.

→ ADVANTAGES :-

→ Smaller in size, easier to fabricate, low cost, low noise device, high resistance to radiation, Internal power consumption is negligiable.

→ Disadvantages :-

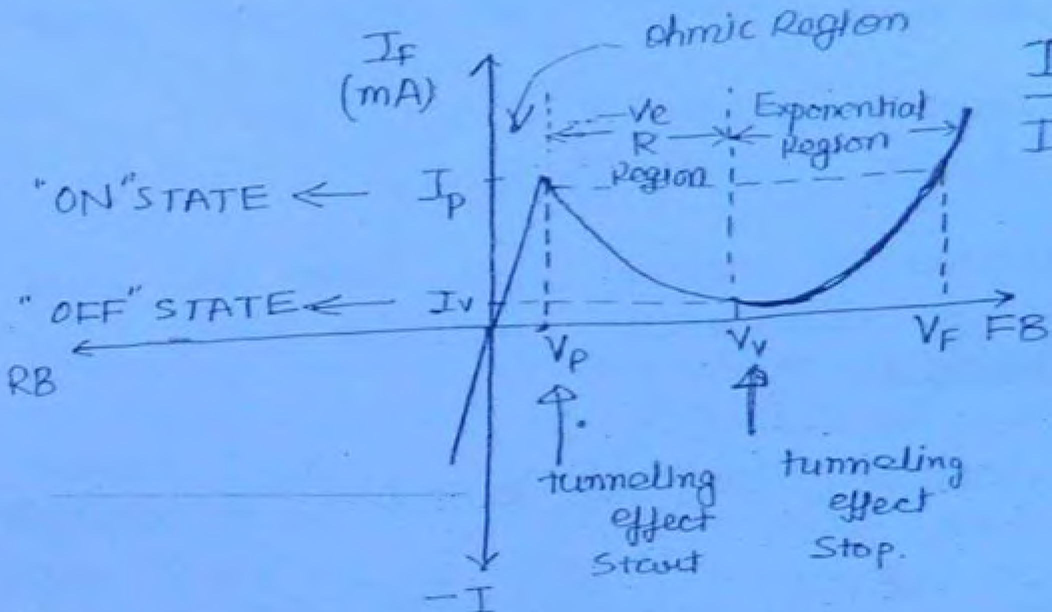
→ It is a two terminal Device and therefore there is no isolation inbetween the o/p section and i/p section.

→ Smaller voltage swing.

Definition of Tunneling effect →

In tunnel Diode the width of Depletion layer is very narrow and is almost equal to 1/50th of wavelength of visible light and therefore the charge carriers will be penetrating to the Depletion layer almost at the speed of light and this quantum behaviour of the charge carriers is called tunnelling effect.

VI characteristics of tunnel Diode :→



I_P = Peak current
I_V = Valley current

→ A RB tunnel Diode is a resistor.

→ when Tunnel Diode is RB the current is linearly increasing with the voltage and the device now working as a linear device i.e. a resistor.

→ In exponential Region tunnel diode will be working as normal Diode

→ Tunnel Diode generally operated in −ve resistance region.

→ The operating point or Q-point of tunnel Diode is located at the centre of −ve resistance region.

→ In tunnel Diode −ve resistance mean as forward voltage increases the forward current decreases

→ The −ve resistance of tunnel diode is due to tunneling effect.

→ Tunnel Diode will exhibit -ve resistance property when device changes its states from ON to OFF.

→ In tunnel diode cuin voltage is zero.

→ Tunnel diode will exhibit -ve resistance property when :→

① FB :→ changes from V_P to V_B

② FC → changes from I_P to I_V.

→ Negative resistance of tunnel diode can be used in designing of microwave oscillator and relaxation oscillator.

→ For a good tunnel diode, the essential requirement is :→

→ larger I_P/I_V ratio

$$\frac{I_P}{I_V} = 15\,(GaAs),\; 7.5\,(Ge),\; 2.5\,(Si)$$

→ Tunnel diode can be fabricated with GaAs or with Ge material and never with the Si material.

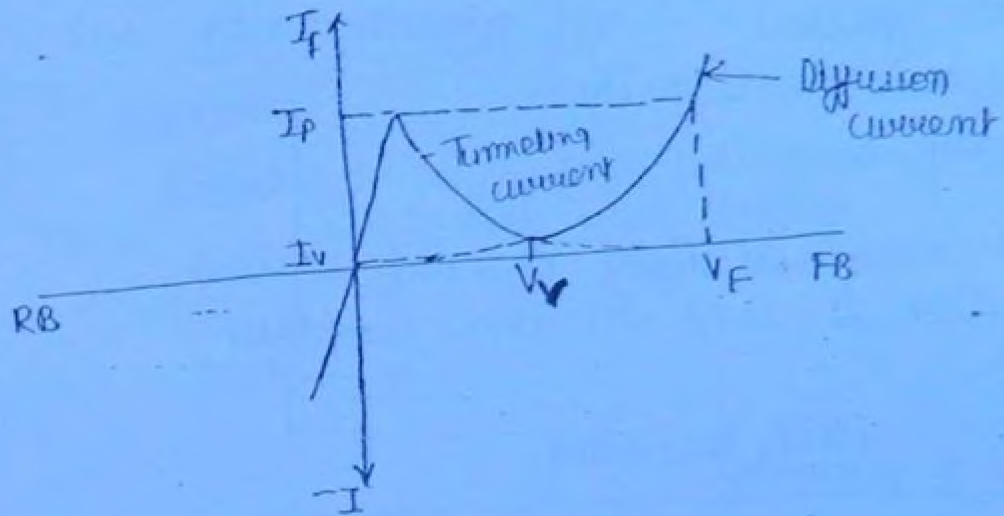
→ High quality tunnel diode are made with GaAs.

→ Commercial tunnel diode are made with Ge.

→ Tunnel diode exhibits multifeature property or triple valued property. (i.e. any value of forward current between I_V & I_P can be obtained with three different sets of forward voltages and this property is used in designing of pulse circuit and industrial applications)

→ Tunnel Diode is also used as PARA-Amp^r. (i.e. as a parametric amp^r and it is microwave power amp^r used with satellite communication).

→ Parametric characteristics :-



→ Tunnelling current is maximum at peak point

→ Tunnelling current is minimum at valley voltage.

→ Beyond valley voltage tunnelling current reduces to zero

→ Diffusion current is small at valley point.

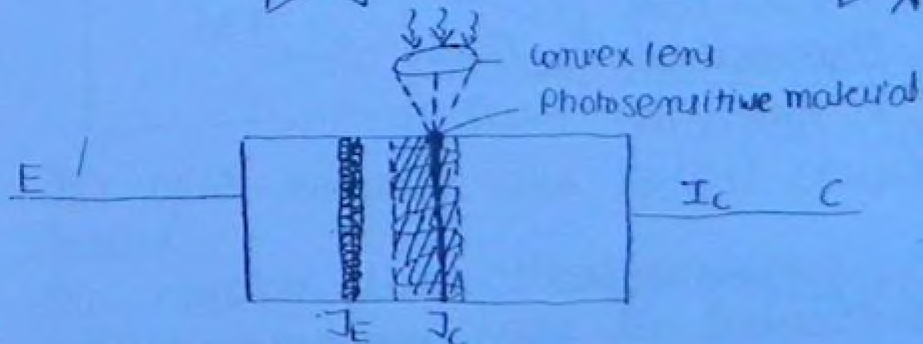
→ Above valley voltage diffusion current exponentially increases with the forward voltage.

→ Diffusion current is large at peak point.

PHOTOTRANSISTOR :→ Photo-Duo-Diode.

→ Principle → photoconductive effect. ☆

→ Symbol -



→ Collector junction i.e J_C is made photosensitive

(NOT IMP)

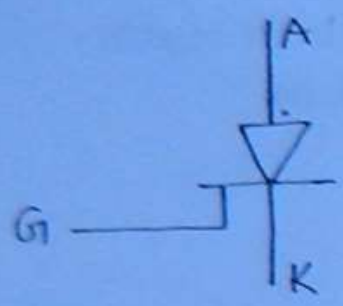
Thyristors.

- Power switching Device.
- Can handle large amount of power with negligiable internal power consumption.
- Fabricated only with Si.
- Ge Thyristor are not practical.
- Bistable Device.
- Basically a latch i.e. a device having ON state and OFF state which are highly stable
- Basically a multilayer semiconductor device.
- can be unidirectional or bidirectional.
- Can be voltage operated or current operated or suitable for both.
- When thyristor changes states from OFF to ON due to applied voltage, it is called voltage operation
- When a thyristor changes its states from OFF to ON becoz of applied current it is called current operation
- Thyristor are faster then BJT.
- Thyristor family members are

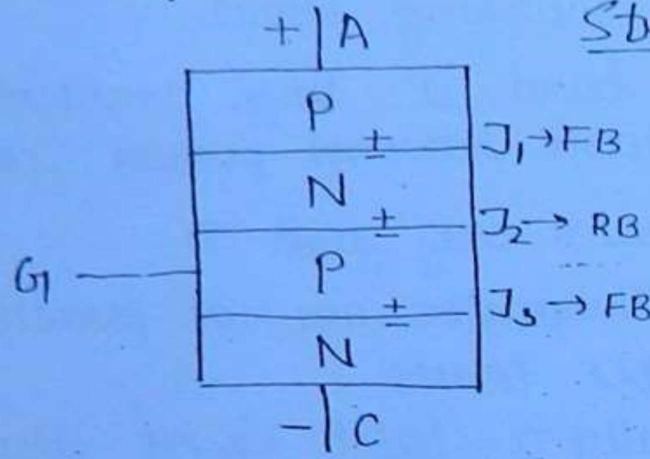
  SCR
  SCS
  SUS
  SBS
  TRIAC
  DIAC
  PNPN or shottky D
  UJT.

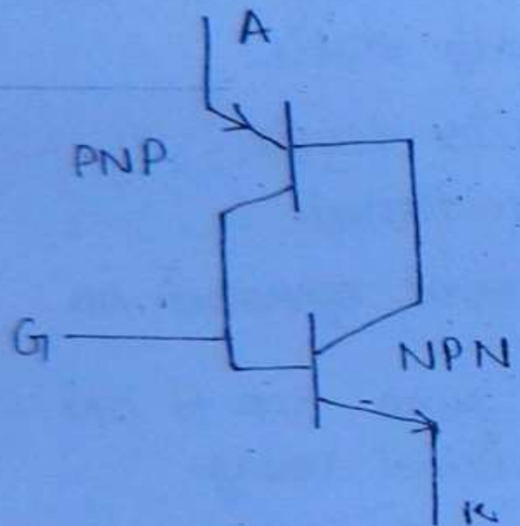
SCR (Silicon Controlled Rectifier) :→

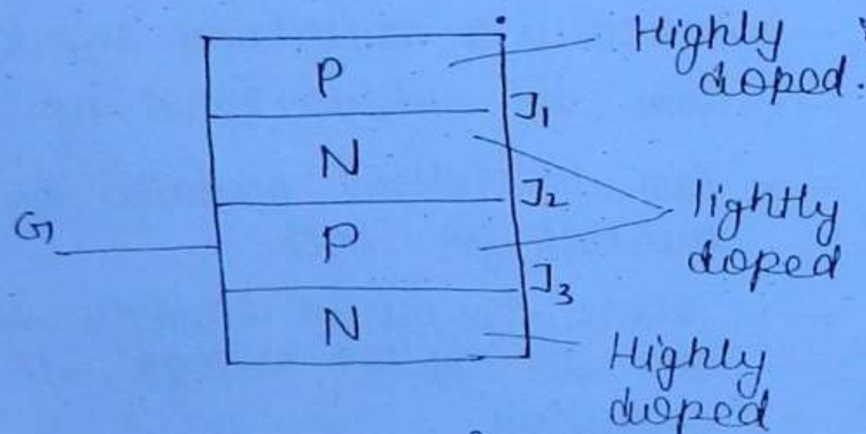
Symbol.



Structure







Equivalent ckt.

→ A three terminal Device having anode, cathode and ~~controlled~~ gate.

→ Four layer solid state device. (SC device) with three junction

→ In SCR gate is made with p-type SC.

→ Unidirectional device (i.e. SCR will be conducting only when anode is +ve with respect to cathode.)

→ If anode is given −ve with respect to cathode then SCR will not conduct.

→ The equivalent circuit of SCR is represented by a transistor latch.

→ In the transistor latch when one transistor is ON the other transistor is OFF.

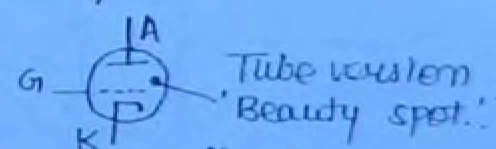
→ The equivalent circuit of SCR is represented by one PNP transistor and one NPN transistor connected such that the collector of first transistor is given to base of second transistor and collector of second transistor is given to base of first transistor.

→ SCR is fast switch.

→ Switching time nsec (10^{-9}).

→ The tube version of SCR is thyratron

→ Thyratron is a gas triode



→ SCR is a controlled Rectifier. (i.e. the duration of anode current can be controlled).

→ SCR can be used in poly-phase rectifiers.

→ SCR can be fabricated with
① Planar technology.
② MESA Technology.

→ SCR is generally specified in terms of breakover voltages. (V_{BO}) → 50V to 1800V.

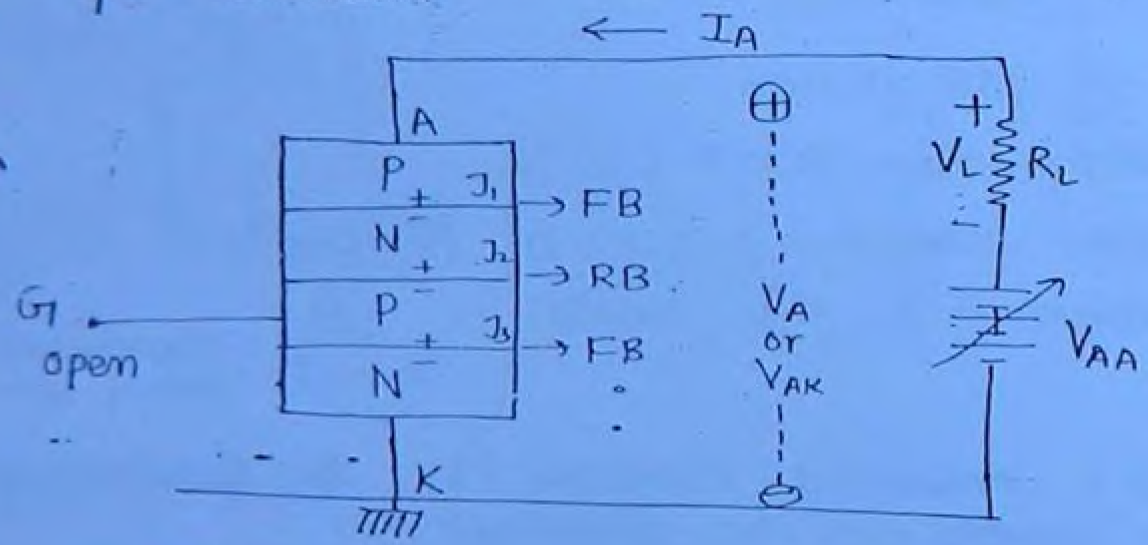
→ SCR is always operated under FB.

→ When SCR is FB with a voltage less then V_{BO} then junction J_1 & J_3 are forward biased and J_2 is RB. Hence internal resistance of SCR is greater then 1 MΩ. and it is in OFF state i.e. Non-conducting.

→ OFF state is also called <u>forward Blocking state</u>.

→ <u>Voltage Operation of SCR</u> :→

→ Under voltage operation of SCR the gate is kept open circuited.



$$V_L = -I_A R_L$$

<u>let $V_{AA} < V_{BO}$</u>, the junction J_1 & J_3 are FB & J_2 is RB, and the internal resistance of SCR will be greater then 1 MΩ Hence anode current is zero & SCR is not conducting i.e it is in the OFF state.

→ When V_{AA} gradually increases junction J_2 moves more reverse biased

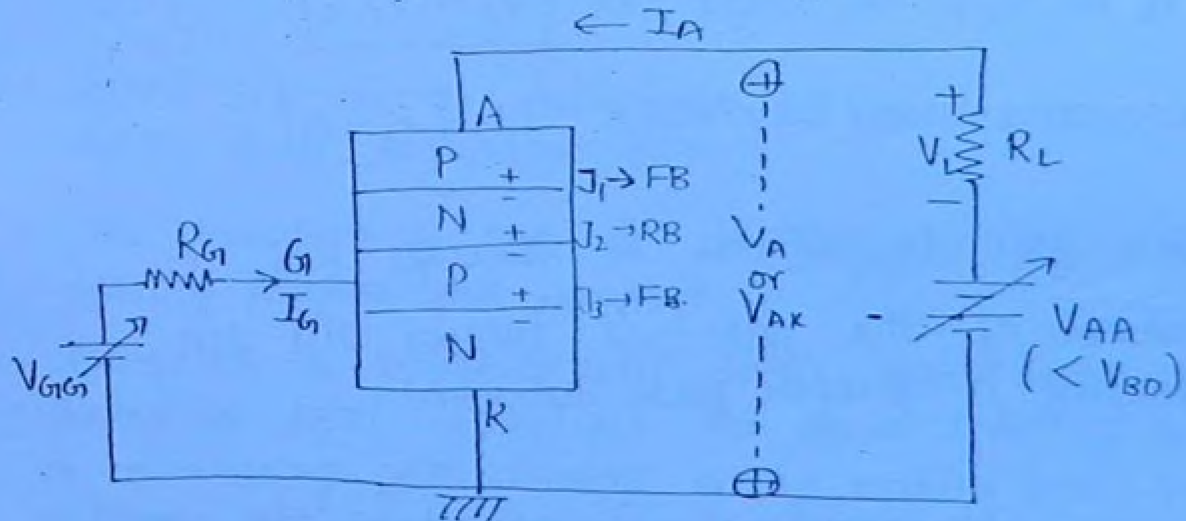
→ When anode supplied voltage $V_{AA} = V_{BO}$ the RB junction J_2 will enter into breakdown and a large anode current is flow & SCR is in the ON state.

→ SCR can be switched OFF by decreasing V_{AA} so that the anode voltage just falls below V_H (Holding voltage) and SCR is switched off.

→ The main disadvantage of voltage operation is we require anode supplied voltage equal to V_{BO} to operate the device.

Current Operation of SCR. :→

→ Also called gate operation of SCR.



$$I_G = \frac{V_{GG} - V_\gamma}{R_G}$$

$$I_G = \frac{V_{GG} - 0.7}{R_G}$$

→ The SCR can be switched OFF by using any one of following three technique :-

(1) By disconnecting the power supply.

(2) By giving anode negative w.r.t. to cathode.

(3) By reducing anode supply voltage so that the anode current falls below holding current (I_H). then SCR is OFF state.

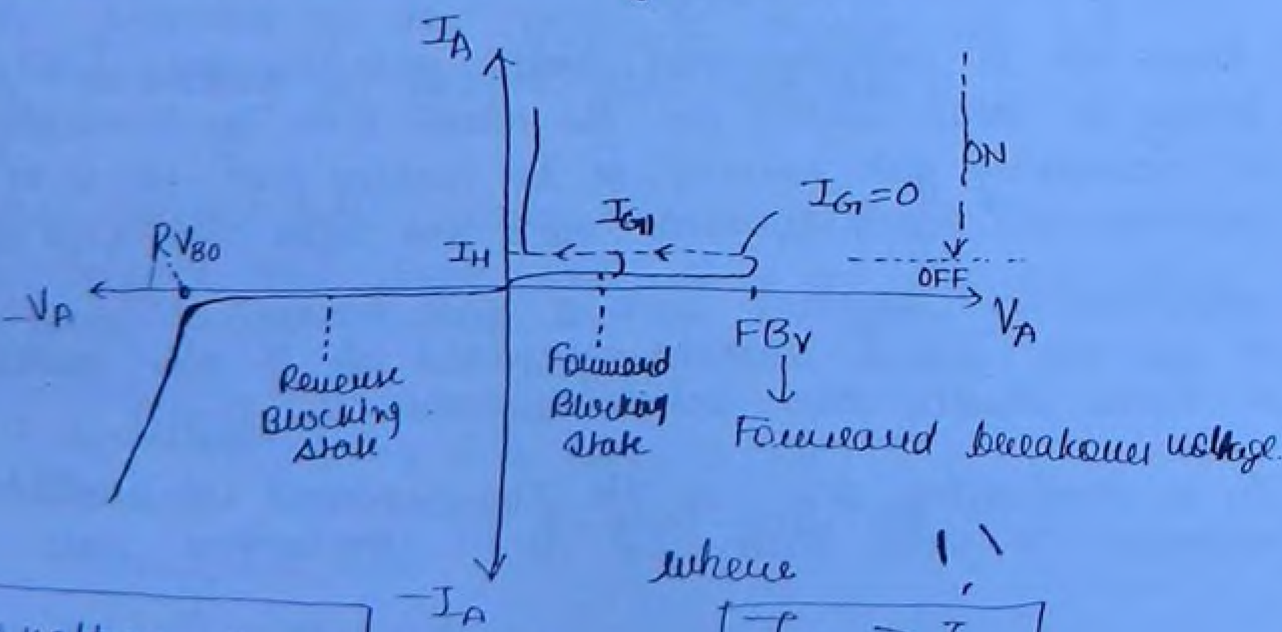
(Low current knock out Technique).

→ if $I_A > I_H$, SCR is in ON state.

→ If $I_A < I_H$, SCR is in OFF state.

→ when SCR is switched OFF, the gate terminal will be regaining its control on the device.

VI characteristics of SCR :→



Firing voltage of SCR $\propto \frac{1}{I_{G1}}$

where $I_{G1} > I_{G0}$

→ By applying larger gate currents we can fire the SCR with smaller anode supply voltages.

→ The main advantages of current operation is we can fire the SCR with smaller anode supply voltage then its breakover voltage

→ Technical data :-

(1) SCR can handle power upto 50 MW

(2) Breakover voltages are in range of 50 V – 1800 V

(3) Switching time n sec

(4) max. power. dissipation 1 W

(5) SCR can handle current upto 2000 A.

Holding Current (I_H) :→

It is the minimum anode current required to keep the SCR in the ON state.

Holding current is very sensitive to temperature.

I_H decreases with increase in temperature.

LATCHING CURRENT (I_{Latch}) :→

It is the minimum gate current required to trigger to SCR so SCR goes to the ON state.

latching current typical value is 1 mA.

In SCR Holding current < Latching current

Turn-on-time (t_{ON}) :→

It is the time required to switch on the SCR.

t_{ON} increases with temperature.

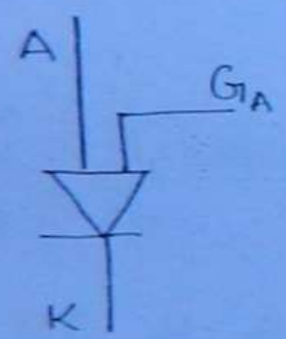
t_{ON} increases with anode current.

turn-off time (t_{OFF}) :→

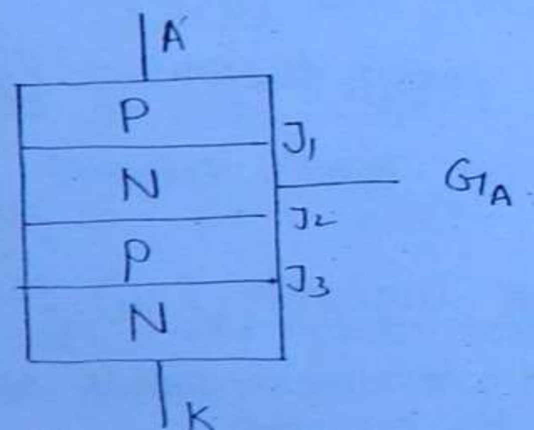
It is the time require to switch off SCR.
turn-off time increases with temperature.
t_{OFF} increases with anode current.

→ SCR can be used to speed control of DC motor.

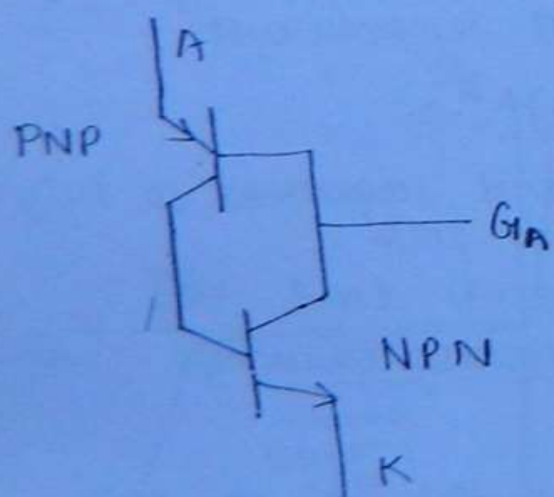
SUS (Silicon-Unilateral switch) :→



Symbol.



Structure



→ equivalent Circuit.

→ 3- terminal device having anode, cathode and anode gate

→ Four layer device with 3-junction.

→ Unidirectional device.

→ Current operation is more popular.

→ Equivalent circuit is a transistor latch.

→ In SCR gate is p-type SC & therefore it is +ve triggered.

→ In SUS gate is N-type SC and therefore it is negative triggered

→ Popularly known as complementary SCR (CSCR).

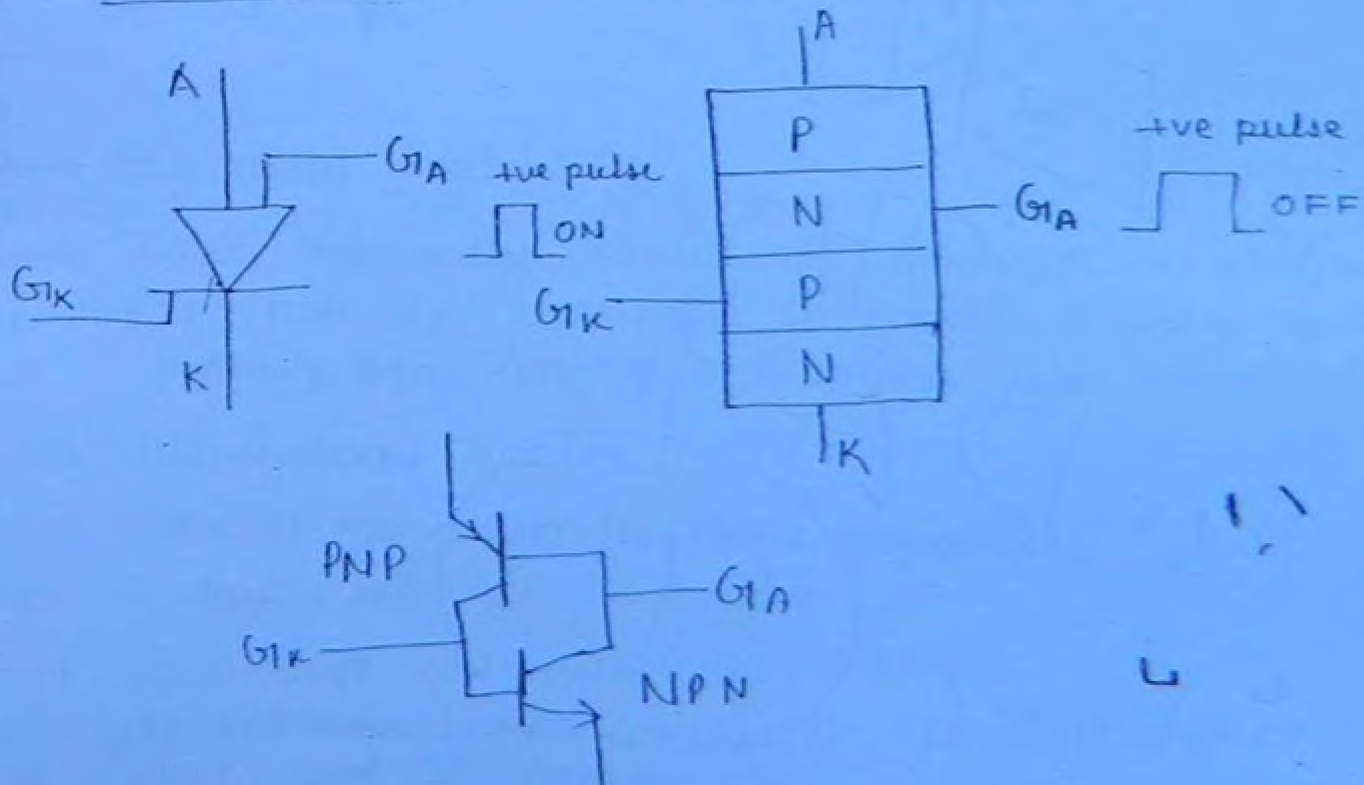
→ Characteristics are similar to SCR.

→ SUS can be used as

(1) As a relaxation oscillator.

(2) As a PUT (Programmable unijunction Transistor).

SCS (Silicon Controlled Switch) :→



→ Four terminal device (Anode, cathode, cathode gate and anode gate) :

→ Unidirectional device.

→ Current operation is more popular.

→ Four layer device with 3 - junction.

→ Equivalent circuit is given by transistor LATCH.

→ Also known as "SCR with two gate"

(or)

"Low current SCR with 2 gate"

(or)

"Low current SCR with Additional gate"

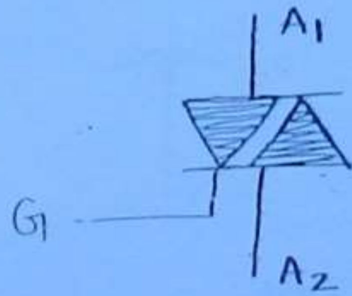
→ characteristics & application are similar to SCR.

→ SCS can be operated with eigther gate terminal and with eigther pulse.

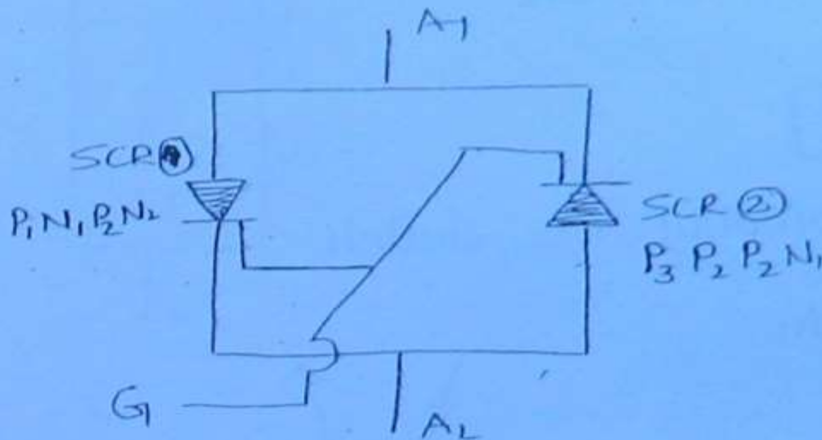
END OF DAY

TRIAC

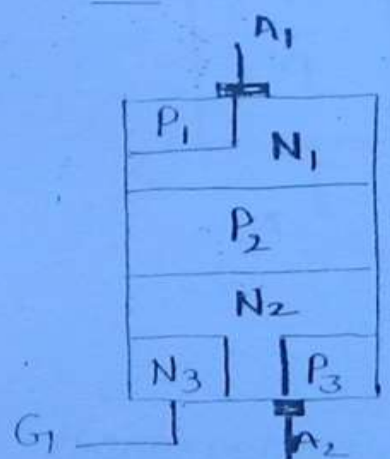
→ Three terminal AC switch

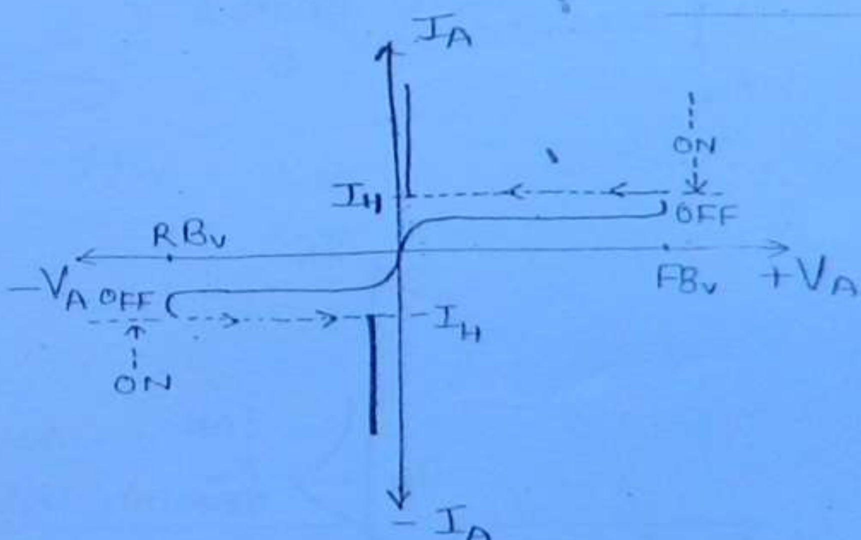


symbol



structure





→ Also called Dual SCR

→ Triac Internally consist of two SCR in antiparalle (i.e. two SCR connected in parallel & with opposite polarity and having a common gate terminal)

→ Bidirectional Device

→ Current operation is more popular

→ 5 layer solid state device

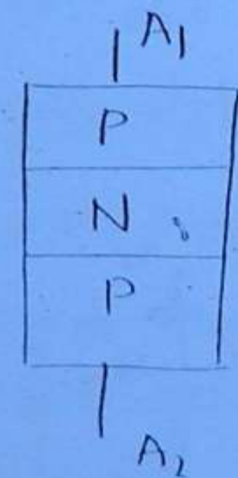
→ Equivalent ckt consist of 2 SCR.

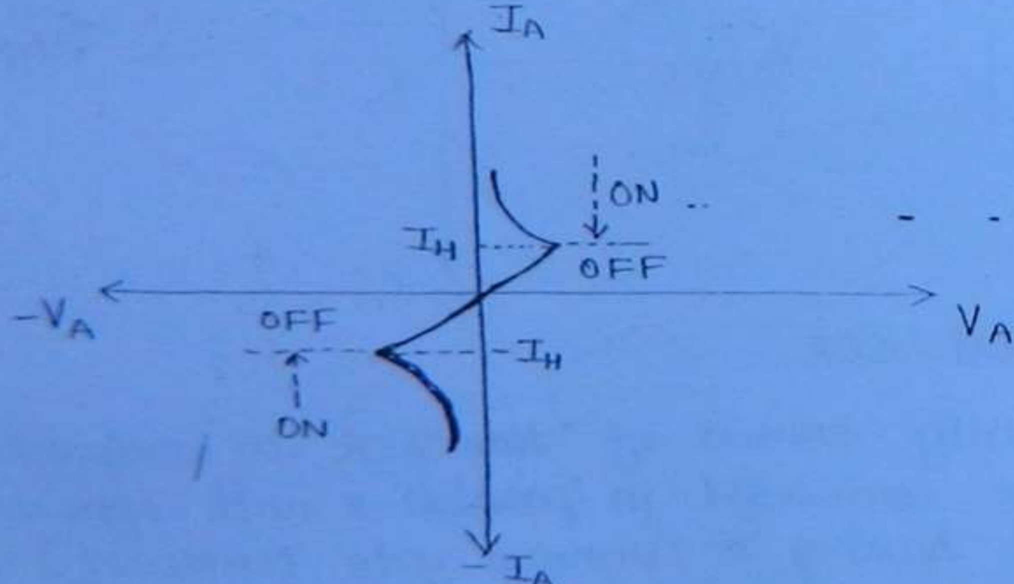
→ characteristics are similar to SCR but deflected in first and III quadrant used for speed controller AC motor.

→ Triac can also be used for designing of inverter circuit.

DIAC

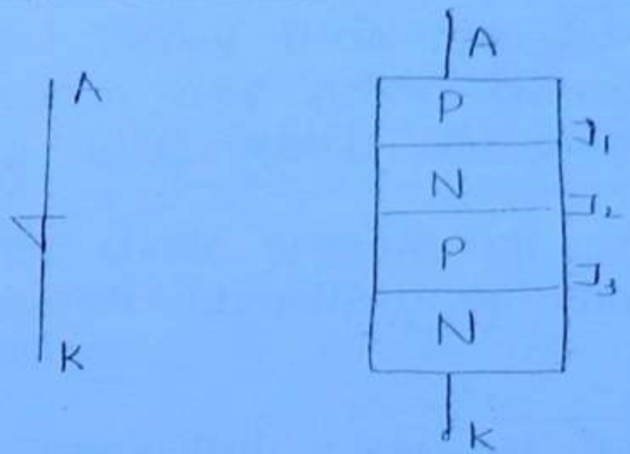
→ Two terminal AC switch.

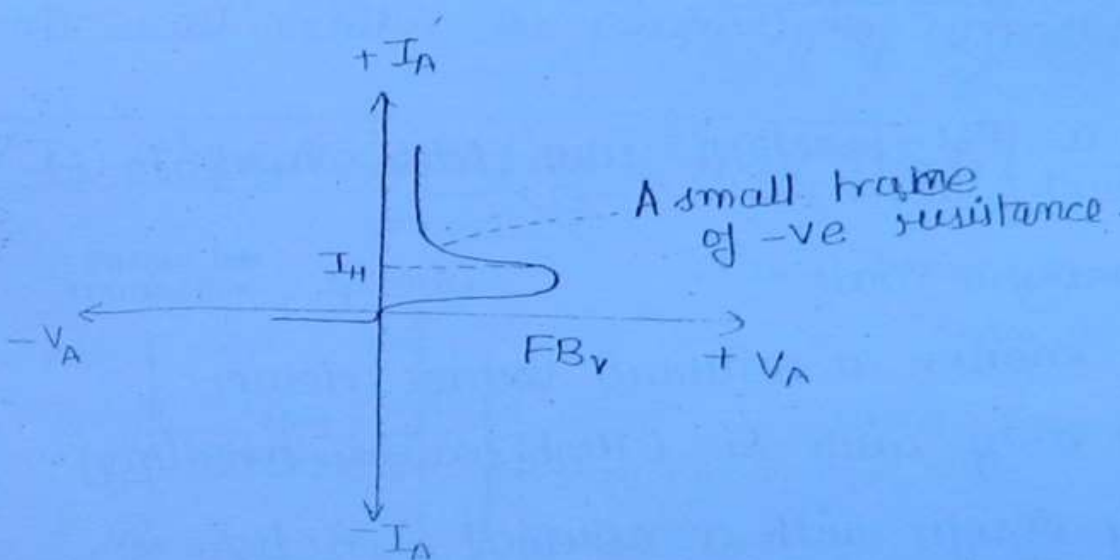




→ Bidirectional device.
→ Only voltage operated device.
→ Three layer solid state device.
→ Widely used to trigger the SCR.

PNPN DIODE or Schockley Diode





→ Unidirectional device

→ Only voltage operated device

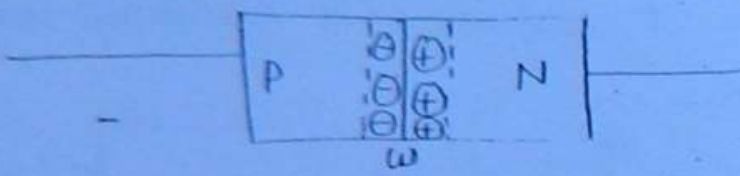
→ Four layer solid state device with 3 junction

→ Also called four layer diode

→ characteristics denotes a small trace of -ve resistance but it cannot be used for any practical application so shockley diode cannot be considered as a -ve resistance device.

→ Major applications as a power diode

ZENER DIODE :→



→ Basically a PN junction with little increase in doping level (1 : 10^5)

→ A Breakdown diode.

→ Popularly known as constant voltage device.

→ Fabricated only with Si (High power handling)

→ Generally design with a normal junction

→ Major applications is as a voltage regulator circuit

→ Can be used as reference voltage device

→ Always operated under reversed biased.

→ Zener diode is specified in terms of breakdown voltage ($P_{Z max}$)

→ Zener diodes are available with breakdown voltages in the range 2.5V to 300V.

→ When forward biased it will be working as a normal diode

→ cutin voltage is 0.7 V

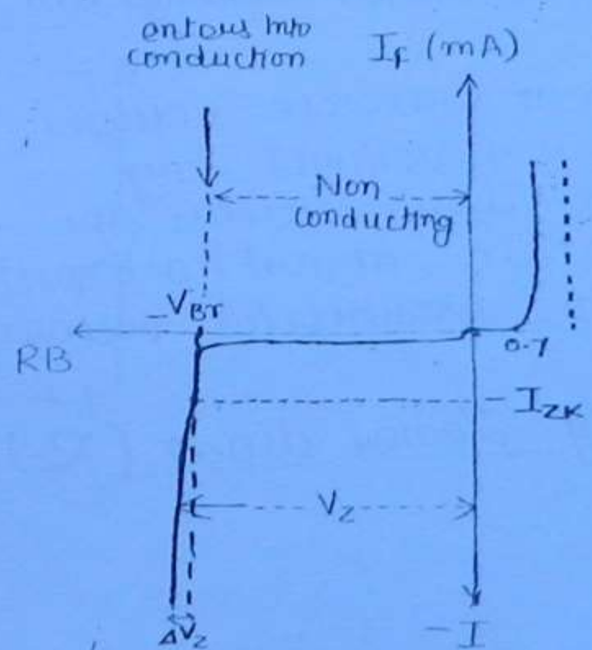
→ latest zener diode are fabricated with abrupt junction and when operated under reverse biased, they will exhibit the property of tunnelling effect.

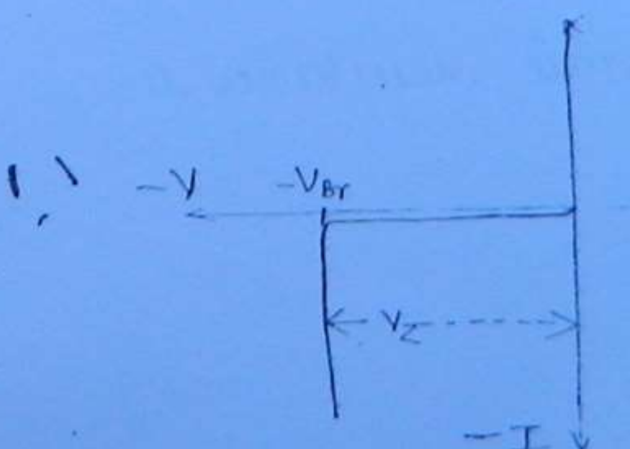
→ Zener diode operate on the principle of tunnelling effect or tunnelling of charge carriers across the junction

→ A zener diode operated in voltage regulator circuit will exhibit the property of tunnelling effect.

VI characteristics of Zener Diode :→

I_{ZK} = Zener Knee Current or Mean I_Z.





VI characteristics of ideal ZD

- When zener diode is Reverse biased with a voltage below the breakdown voltage. The current is practically zero and zener diode is non-conducting and at present it will be working as a normal diode

- When reverse voltage equal breakdown voltage the current suddenly increases to I_{ZK}. and this is due to breakdown phenomenon

When reverse voltages are greater then breakdown voltage more and more current will be passing through the zener diode but the voltage across the zener diode will be maintain almost a constant and it is around the breakdown voltage.

In Ideal zener diode when reverse voltages are greater then breakdown voltages large current flows but voltage drop across the zener diode will be maintain almost a const. and it is exactly equal to breakdown voltage.

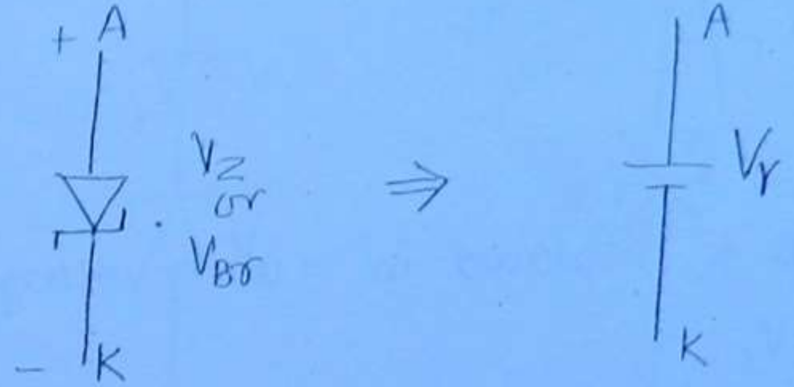
Dynamic Resistance of Zener diode (R_Z). :→

$$R_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

- For Ideal zener diode dynamic resistance is zero

Equivalent Circuit of Zener diode :→

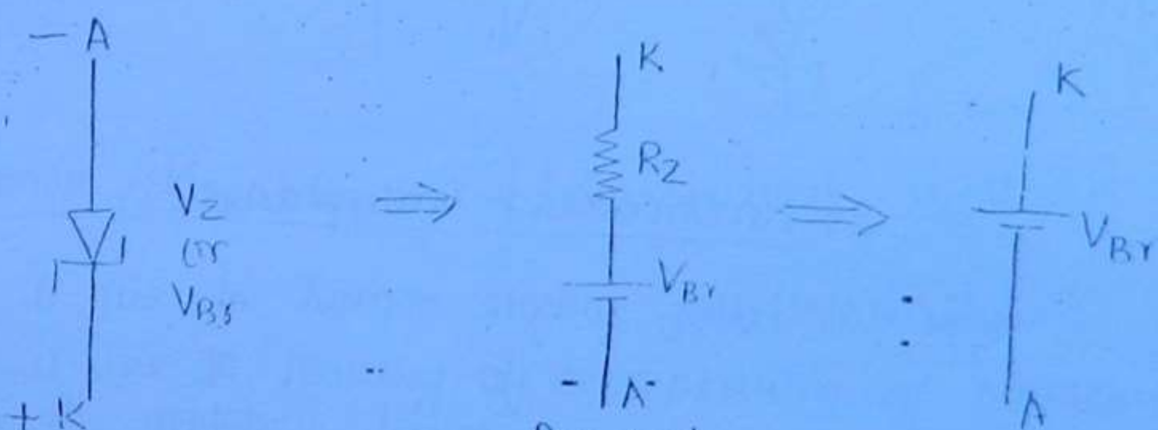
(1) When zener diode is FB :→



V_γ = cut in voltage
0.7 V

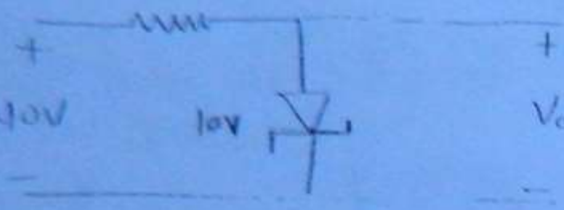
→ A forward biased zener diode is replaced by its cutin voltage.

(2) When zener diode is RB :→



Practical   Ideal

Prob ➡ Find output voltage V_o

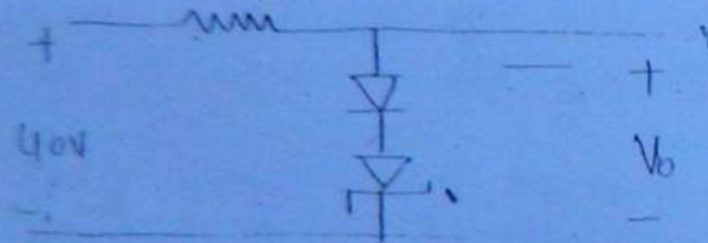


Sol ZD is FB & replaced in cut in voltage

$V_o = V_\gamma$

$V_o = 0.7V$

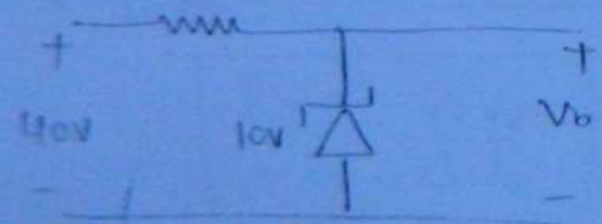
Prob



Si D is forward biased & replaced V_γ

$V_o = 1.4V$

Prob.

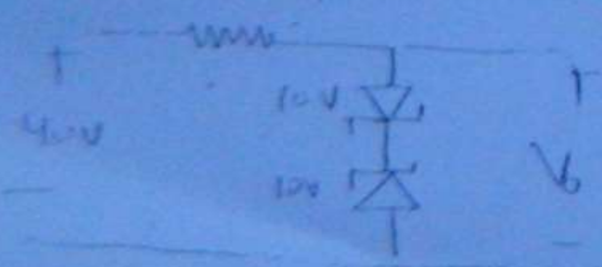


ZD is RB & conducting

$V_o = V_{Br}$

$V_o = 10V$

Sol

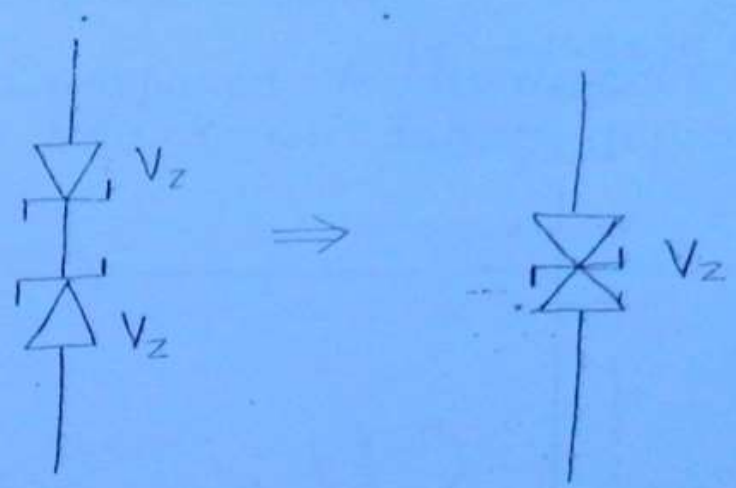


$V_o = V_\gamma + V_{Br}$

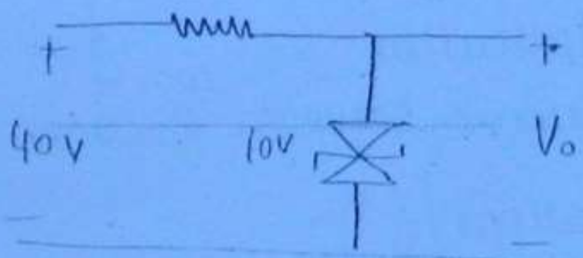
$= 0.7 + 10$

$= 10.7V$

→ When two identical zener diode are connected back to back it can be replaced as given below -



Prob



Ans. (10.7) A

Zener Breakdown Phenomena :→

→ It is due to larger electric field intensity.

→ It is due to tearing off or rupturing of covalent bonds in the depletion layer

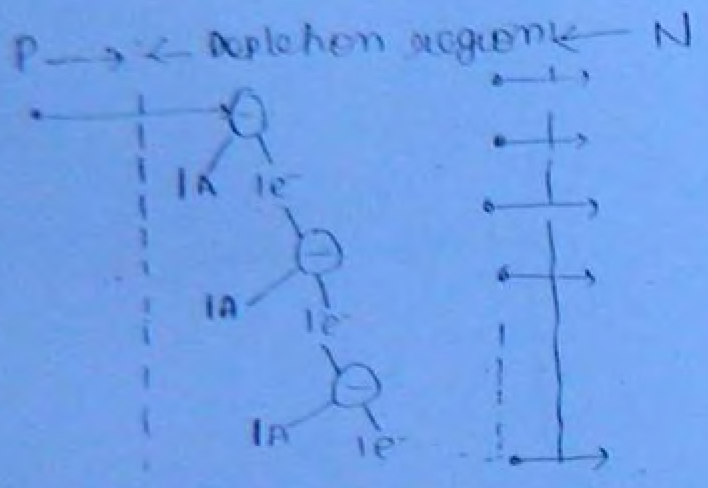
→ Zener breakdown occurs for breakdown voltages below 6 V

→ Zener breakdown voltage decreases with the temperature (NTC)

→ The temperature coefficient for zener breakdown voltage is negative

$$|E| = 2 \times 10^7 \ V/m$$

Avalanche Breakdown Phenomena :→



→ It is due to electron multiplication.

→ It is due to multiple collisions between e⁻ and ions in the depletion layer.

→ It is due to impact ionisation

→ Avalanche breakdown occurs for breakdown voltages greater than 6V

→ Avalanche breakdown voltage increases with temp (PTC)

→ The temperature coefficient for avalanche breakdown voltage is +ve.

Ques → Impact ionisation occurs in Zener diode

→ large flow of current through zener diode is due to flow of minority carriers.

→ if the current passing through ZD is doubled then voltage drop across ZD is almost constant

→ In a highly doped Diode the breakdown is due to ~~Zener~~ Zener effect

$\downarrow V_{Br} \propto \frac{1}{\text{Doping} \uparrow}$

$< 6V$

In a slightly doped diode the breakdown is due to Avalanche effect

→ When compared to avalanche breakdown Zener breakdown higher doping concentration.

FET (Field effect Transistor) :→

→ Operation of FET :- Depends on electric field intensity produced in the channel.

→ Voltage control device VCD

→ Unipolar Device

→ Majority carrier device.

→ No minority carrier

→ less noisy device due to the absence of minority carriers.

→ likeage currents are zero & therefore temp effect on the device is less

→ Excellent thermal stability and this is due to the absence of minority carriers (likeage currents)

→ FET is a having better thermal stability than BJT

→ High input resistance device (> 1 MΩ)

→ Internal power consumption or power dissipation is less

→ Fabricated only with Silicon.

→ When compared to BJT FET is smaller in size and easier to fabricate.

→ Offers a larger bandwidth and therefore reproduction of input signal is excellent

→ Gain bandwidth product is a constant

→ offset voltage is zero.

→ FET is used as an excellent signal chopper and this is due to zero offset voltage.

Disadvantages of FET :→

→ Offers smaller gain

→ low gain bandwidth product

→ As compared to BJT FET is better device

→ FET is an excellent amplifier at low frequencies and high frequency.

→ Source → It is source of majority carriers or it is terminal by which majority carrier will be entering into the device

→ Drain → In drains of majority carriers. It is the terminal by which majority carriers will be leaving the device

→ Gate → It is terminal which controls majority carriers moving from source to drain or indirectly control the drain current

Channel → It is the space in between the two gates.

→ BJT is assymmetrical device and therefore emitter and collector terminal cannot be practically interchange.

→ FET is symmetrical device and therefore source and drain terminal can be interchange practically.

Classification of FET.

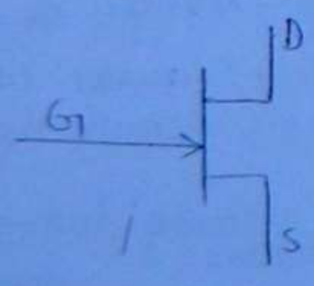
① JFET

(Junction field effect transistor).

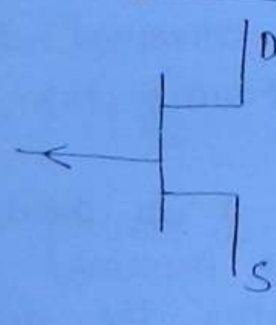
→ Three terminal Device (S, G & D)

→ $R \Rightarrow 10^6$ to $10^8 \Omega$

→ (i) N- channel JFET. :-



(ii) P- channel JFET



(2) MOSFET (Metal oxide Semiconductor FET)

or

IGFET (Insulated gate FET).

or

MOST (Metal oxide semiconductor transistor)

or

(Metal oxide Silicon transistor)

- → 4 terminal Device [S, G, D and SUB (substrate)]
- → $R_i = 10^{10}$ to $10^{15}\,\Omega$
- → Highest input resistance device.

(i) Depletion MOSFET

- → There will be preexisting channel between source and drain regions
- → Suitable to operate in Depletion and enhancement mode
- → Also called DE-MOSFET

DE-MOSFET → n-channel, p-channel

(ii) Enhancement MOSFET

- → There is no preexisting channel & channel has to be created by applying proper gate to source voltage.
- → Suitable to operate only in the enhancement mode
- → E-only MOSFET

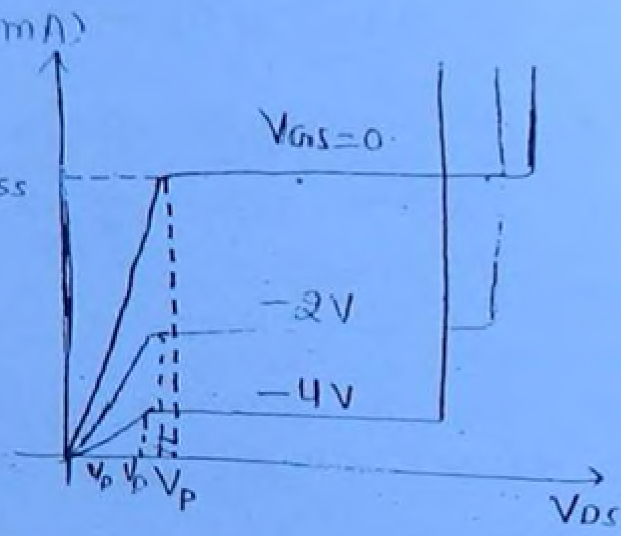
E-only MOSFET → n-channel, p-channel

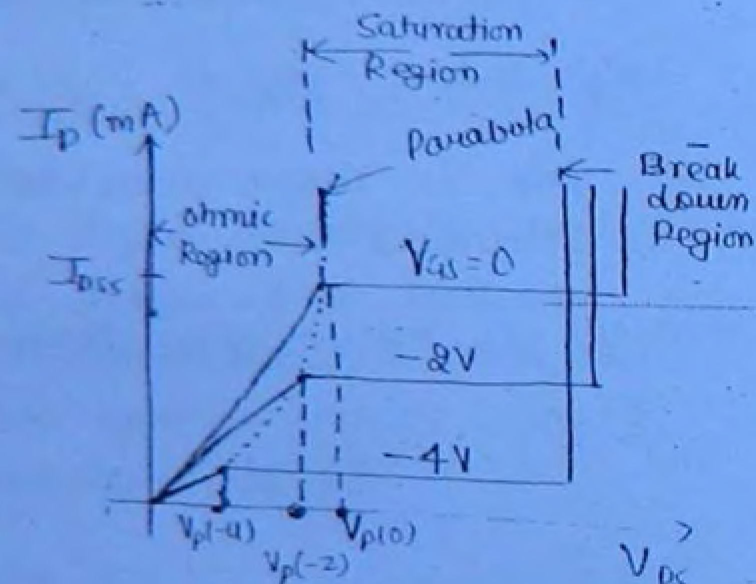
- → R_i of MOSFET > R_i of FET
- → P_D of MOSFET < P_D of FET

→ Step ② By keeping V_{GS} constant & by varying V_{DS} - O/p characteristics or Drain characteristics

I_D V_S V_{DSS}

V_{GS}





→ The drain characteristics of FET is called constant current characteristics (and it is similar to collector characteristics of common - base transistor)

→ FET can work as a constant current source

→ FET is voltage control current source (VCCS)

→ Common base transistor is current control current source (CCCS)

→ Breakdown voltage is a function of V_{GS}

→ Breakdown voltage is maximum when V_{GS} is kept zero

* → In FET breakdown is due to Avalanche effect.

→ In ohmic region FET will work as a linear device i.e as a resistor e.g. VVR (Voltage variable Resistor) or VDR (Voltage Dependent Resistor)

→ In JFET channel behaves as a resistor

→ In the ohmic region by varying gate to source voltage, FET can work as a VVR

→ In the saturation region FET will work as;-

(1) As an amplifier

(2) As 'ON' switch

→ Saturation region is also called current saturation region or pinch-off region

* → FET is generally operated in the saturation region

* → FET is generally operated with $V_{DS} > V_P$

→ Pinch-off Voltage :→ (V_P)

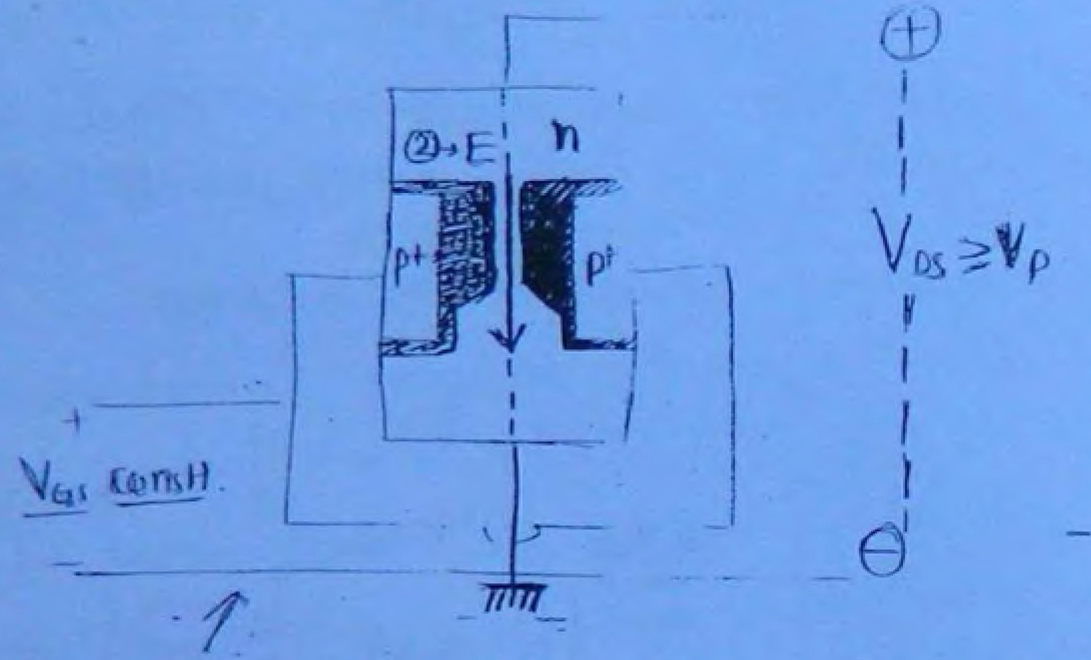
→ It is the minimum value of V_{DS} required where I_D enters into saturation

→ The maximum pinch off voltage is $V_P(0)$ or V_{P0}

→ Pinch off voltage is function of V_{GS}

→ In JFET when V_{GS} is applied, pinch off voltage decreases

→ The locus of $V_P(0)$ corresponds to parabola



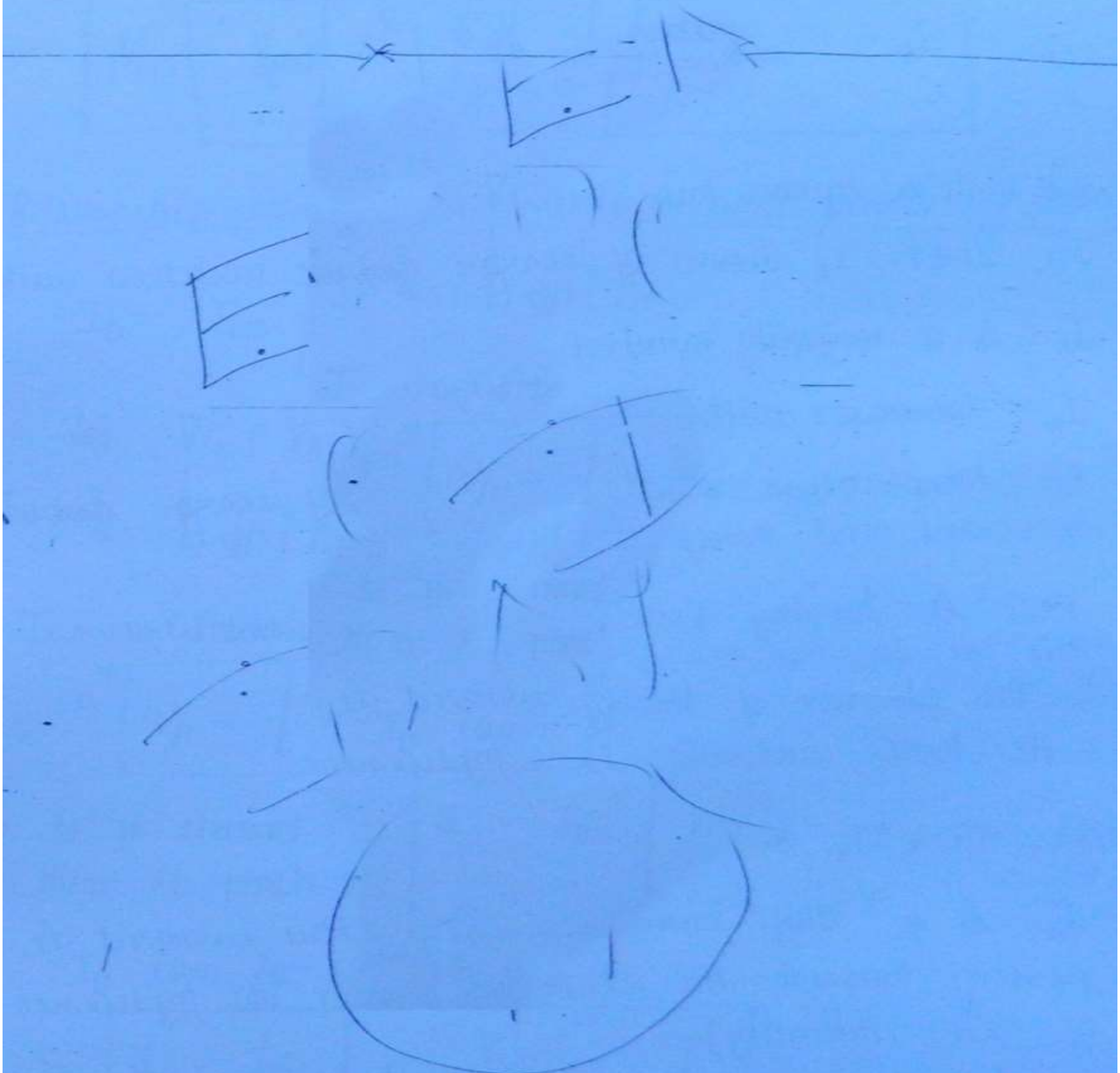
→ **During pinch-off** ① the two depletion layer will be coming extremely closer but they will not keep touching with each other the positive ions in depletion layer of the n-channel JFET will produce a repulsive force & due to this repulsive force the two depletion layer will not being touching each other

→ ② During the pinch off as V_{DS} is increasing above V_P, the two depletion layer will be penetrating more into the channel and they will be try to touch each other but at the same time field intensity will become very large near the drain it is pointing towards the source due to field intensity the two depletion layer are unable to touch each other

③ During the pinch off the ~~deple~~ channel width is narrow but drain voltage is very high and therefore K.E. of e^- will be increasing hence drain is receiving maximum e^- from channel and drain current ~~[illegible]~~ now is unchanged

The e^- in the channel will now move towards drain with high K.E.

The



Equation for Drain Current (I_D) :-

In the saturation region of FET

$$\Rightarrow \quad I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \text{ Amp}$$

- FET is a square law device.
- In JFET I_D decreases as a parabolic variation with V_{GS}.
- I_D is a majority carrier current.
- I_D decreases with the temperature.
- As temperature increases mobility of charge carrier decreases and therefore I_D decreases.
- FET is having excellent thermal stability and this is due to :-
  (1) The absence of leakage current
  (2) As temp increases I_D decrease
- For 1°C, I_D decreases by 0.7%.
- I_D is a drift current (becoz this current is passing through the channel under the influence of EF intensity)

Equation for V_{GS} :→

→ In the saturation region of FET :→

$$\Rightarrow \boxed{V_{GS} = V_P \left[1 - \sqrt{\frac{I_D}{I_{DSS}}} \right]}$$

Relationship between V_{GS} cut-off and pinch-off voltag

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

let $V_{GS} \equiv V_P$ then $I_D = 0$.

↓ (cond^n for cut-off)

V_{GS} (cut off) [Pinch off voltage].

In n-channel JFET

$$\Rightarrow \boxed{V_P = |V_{GS}(\text{cut off})|}$$

→ In n-channel JFET V_{GS} cut-off is −8 V then it pinch off voltage (V_P) is +8 V

I_D can be written as

$$\Rightarrow \boxed{I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS}(\text{cut off})} \right]^2}$$

→ In the equation for I_D, the polarity of V_{GS} and V_P must have the same sign.

→ Pinch-off voltage is also define as the minimum V_{GS} where I_D is reduced to zero.

→ Pinch off voltage is defined as

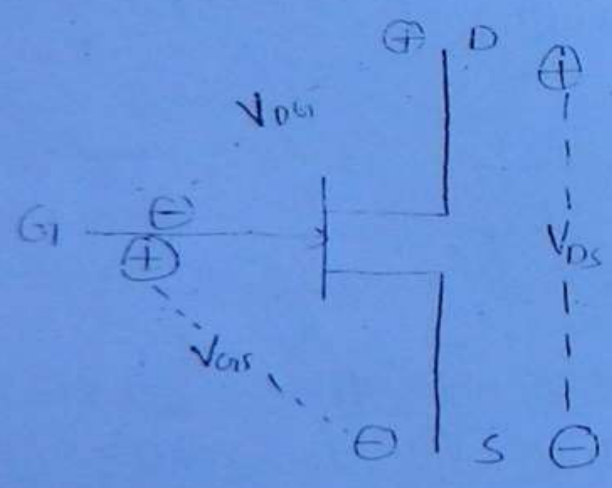
(a) Minimum V_{GS} where I_D is zero. ✓

(b) Minimum V_{GS} where I_D is max.

(c) Minimum V_{DS} where I_D is max. ✓

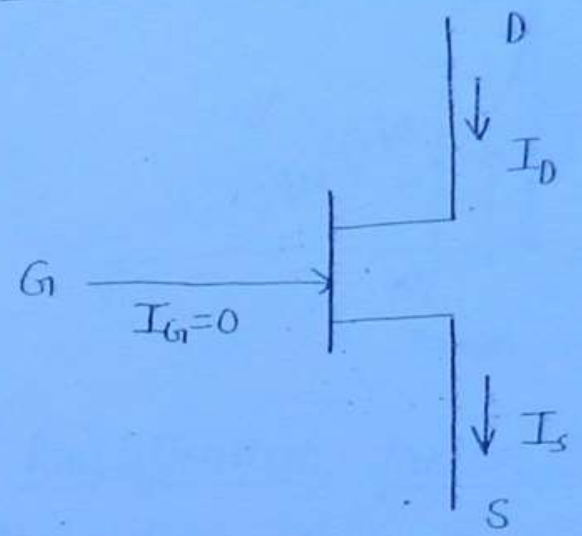
(d) min. V_{GS} where I_D is zero.

Relationship between terminal Voltages of FET :-



$$\Rightarrow \boxed{V_{DS} = V_{DG} + V_{GS}}$$

Source Current (I_S) :→



$$\boxed{I_S \equiv I_D}$$ In magnitude

FET Parameters :→

I_D is a f (V_{GS} and V_{DS})

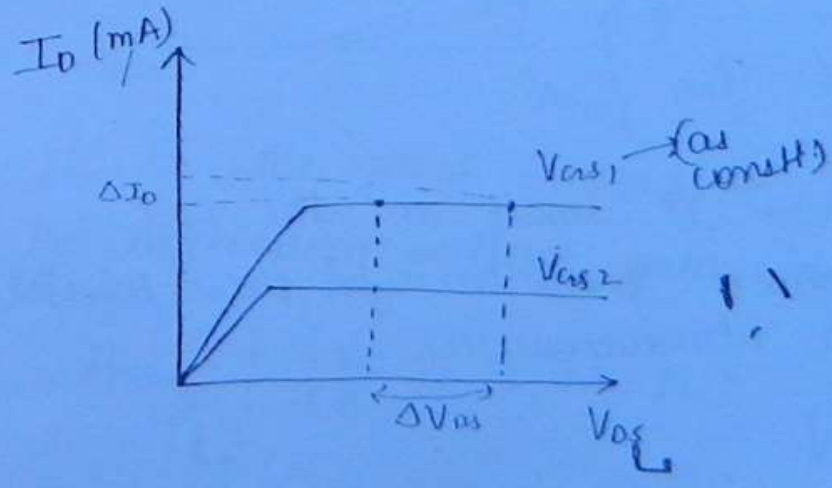
1) Drain Resistance → r_d :→

$$\boxed{r_d = \left. \frac{\Delta V_{DS}}{\Delta I_D} \right|_{V_{GS} = \text{constt}}}$$

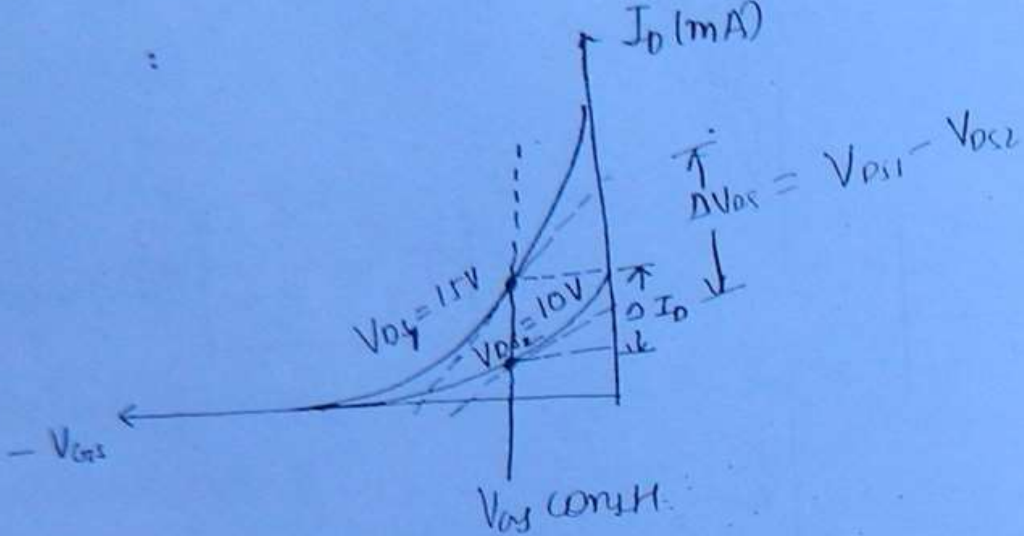
r_d → 10kΩ to 600k

Typ → 500kΩ

r_d is graphically obtained from drain characteristics and transfer characteristic



[for conventional]



→ (b) Trans- conductance → g_m or mutual conductance

$$\Rightarrow \boxed{g = \frac{\partial I_D}{\partial V_{gs}}\Bigg|_{V_{DS}} = \frac{\Delta I_D}{\Delta V_{GS}}\Bigg|_{V_{DS}}}$$

	JFET	MOSFET	BJT
$g_m =$	0.1 mS to 10 mS	0.1 mS to 20 mS	50 mS to 600 mS

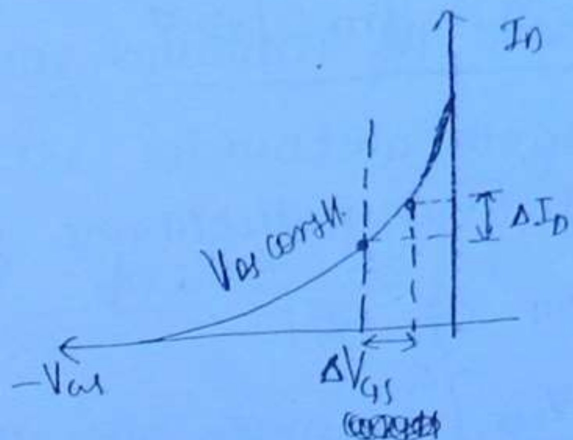
} Not imp. only for ref.

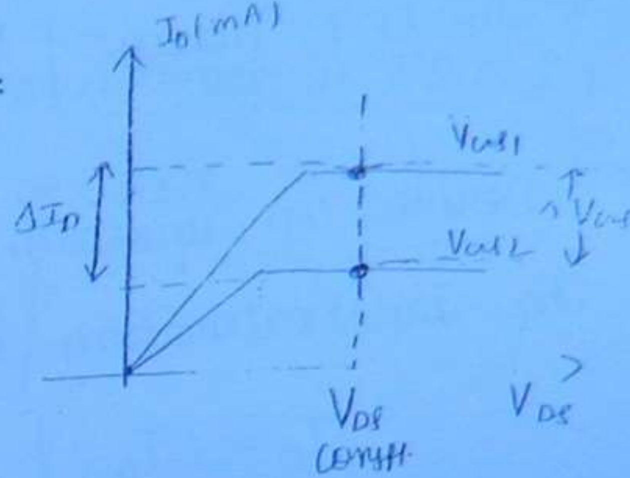
In any device

$$\Rightarrow \boxed{\text{Gain } |A| \propto g_m}$$

→ Since g_m is small, gain is small in the FET

→ g_m is graphically obtained from transfer characteristics and also from drain characteristics





(c) Amplification factor :→ (μ)

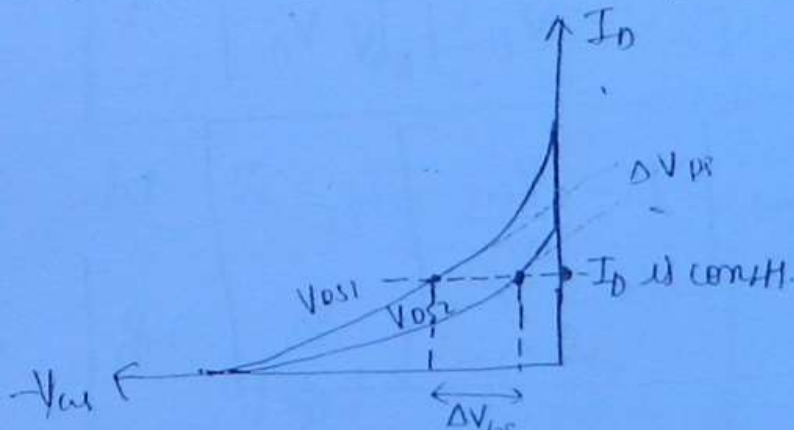
Also called voltage Amplification factor.

$$\Rightarrow \boxed{\mu = -\left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right)\Bigg|_{I_D = \text{constt.}}}$$

μ → 2.5 to 150

μ is always positive value

μ is graphically obtained only from transfer characteristics



→ μ is the most important specification of the FET

→ The maximum voltage gain in the FET is given by μ.

→ $$\mu = -\left(\frac{\partial V_{DS}}{\partial V_{GS}}\right)\Bigg|_{I_D} \quad \text{or} \quad \mu = -\frac{V_{DS}}{V_{GS}}\Bigg|_{I_D = c}$$

→ In FET always $\boxed{\mu = r_d \times g_m}$ ⇒ ☆

Derive an equation for transconductance g_m :-

In the saturation region of FET.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

By- definition

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}}$$

Differentiating the above eq^n w.r.t V_{GS} and keeping V_{DS} const.

$$\frac{\partial I_D}{\partial V_{GS}} = 2 I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[-\frac{1}{V_P}\right]$$

☆

$$\Rightarrow \boxed{g_m = -\frac{2 I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right] \mho}$$

General equation for transconductance in FET :-

In the saturation region of FET

$$g_m = -\frac{2 I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right] \quad \text{---- (1)}$$

from the equation of I_D.

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}$$

Substitute the value in eq (1)

$$g_m = -\frac{2 I_{DSS}}{V_P}\sqrt{\frac{I_D}{I_{DSS}}}$$

$$\Rightarrow \boxed{g_m = -\frac{2}{V_P}\sqrt{I_{DSS} \cdot I_D} \;\; \mho}$$

let $I_D = I_{DS}$

$$\Rightarrow \boxed{g_m = \frac{2}{|V_P|}\sqrt{I_{DSS} \cdot I_{DS}}}$$

if V_{GS} is kept zero in eq (1).

$$\Rightarrow \boxed{g_{mo} = -\frac{2 I_{DSS}}{V_P}}$$

→ g_{mo} is the maximum value of g_m.

↓ value of g_m when $V_{GS} = 0$

$\therefore$ g_{max} occurs when $V_{GS} = 0$ → $g_{max} = -\frac{2 I_{DSS}}{V_P}$.

when $V_{GS} = 0$ then $V_p \longrightarrow V_{P0}$

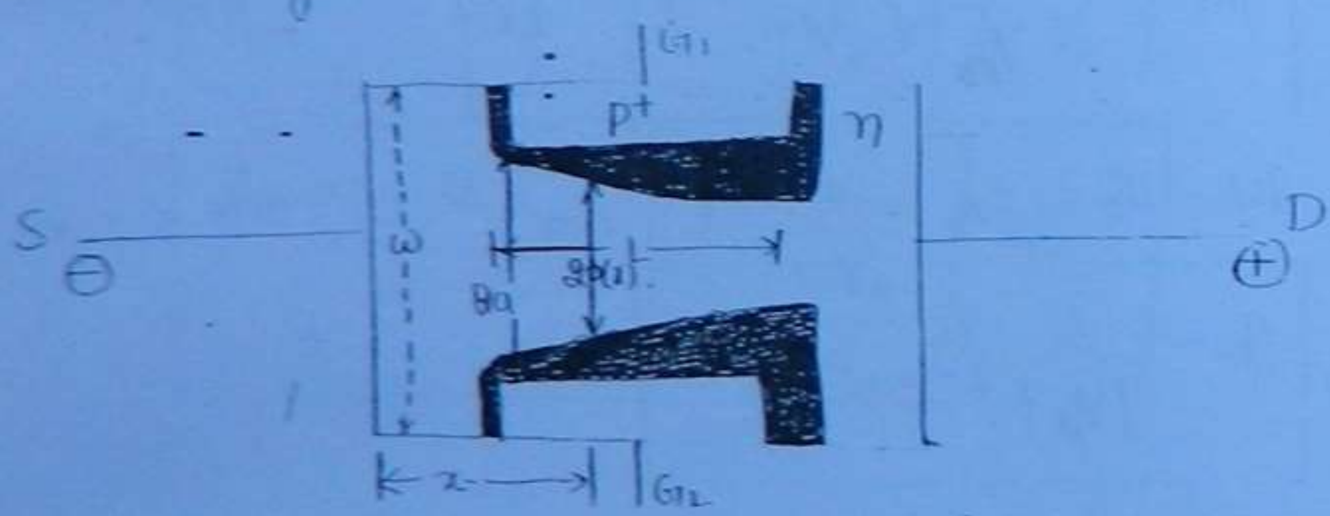
$$\Rightarrow \boxed{V_{P0} = -\frac{2 I_{DSS}}{g_{m0}}} \quad \text{volts}$$

$$\Rightarrow \boxed{g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]} \; \mho$$

$$\Rightarrow \boxed{g_m = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}} \; \mho$$

General equation for JFET :→

considering N channel JFET



→ l is the length of channel

→ w is the width of SC bar.

→ x is distance measured from source end

→ 2a is channel width before the penetration of depletion layer.

→ a is the half channel width before the penetration of depletion layer.

→ 2b(x) is the channel width after the penetration of depletion layer measured at the distance x

→ In n-channel JFET

→ The internal pinch-off voltage is given by :-

IES *

$$|V_P| = \frac{q N_D a^2}{2\epsilon} \text{ volts}$$

→ Drain current

$$I_D = 2b \cdot q N_D \mu_n \left[\frac{V_{DS}}{L/\omega}\right]$$

$$\Rightarrow^* \quad I_D \propto N_D$$

$$\Rightarrow^* \quad I_D \propto V_{DS}$$

$$\Rightarrow^* \quad I_D \propto \frac{W}{L}$$

Drain to source resistance r_{ds}

$$\Rightarrow \boxed{r_{ds} = \frac{V_{DS}}{I_D}}$$

↓

$r_{d(ON)}$ (channel Resistance)

★ $$\boxed{r_{ds} = \frac{L}{2bq\mu_n N_D\, w}}$$

★ $$\boxed{r_{d(ON)} \propto \frac{L}{w}}$$

$r_{d(ON)} \rightarrow 100\Omega$ to $100k\Omega$

$$V_{po} = V_{bi} + V_p$$

$$V_{bi} = V_T \log_e \frac{N_A N_D}{n_i^2} \text{ volt}$$

[for gate exam]

$r_{d(on)}$ is important parameter in the switching application of FET.

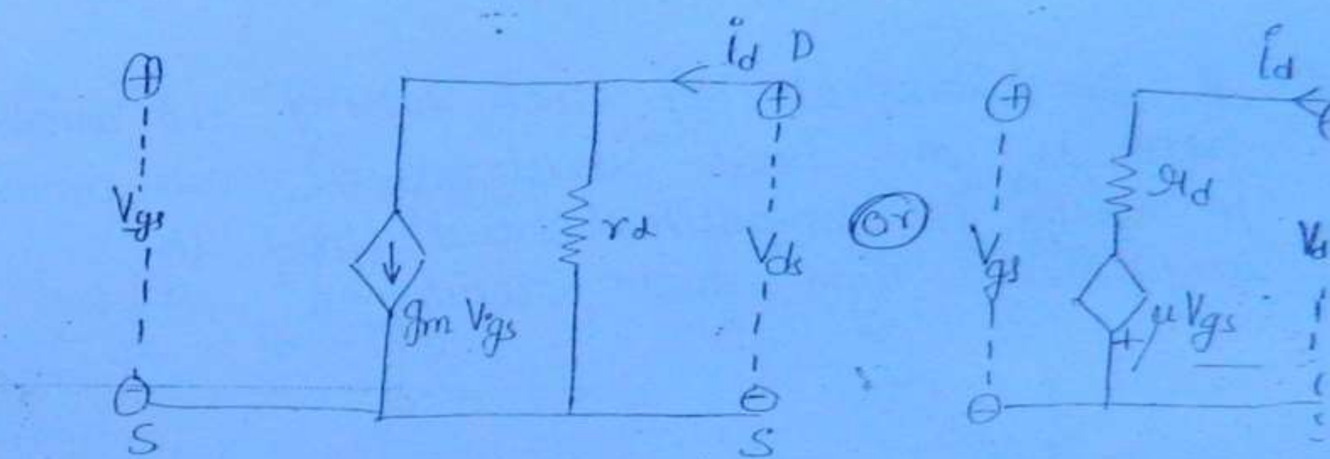
Input resistance of BJT is less then $r_{d(ON)}$

$$\Rightarrow \boxed{R_i \text{ of BJT} < r_{d(ON)}}$$

Equivalent Circuit of FET (JFET & MOSFET) :-

→ It is also called low frequency and small signal equivalent circuit of the FET.

→ It is also called AC equivalent circuit.



→ The above circuit is used to calculate voltage gain and output resistance of the FET amp^r

---

Prob. What is the maximum voltage gain obtain from FET having $g_m = 5mS$ & $r_d = 10K\Omega$ the max.

soln

$$\mu = r_d \times g_m = 50$$

Prob What is the maximum g_m of JFET having $I_{DSS} = 8mA$, $V_p = -4V$

soln

$$g_{max} = -\frac{2I_{DSS}}{V_p} = -\frac{2 \times 8 \times 10^{-3}}{-4} = 4\,m\mho$$

Prob Calculate the g_m of FET having $I_{DSS} = 8mA$, $V_p = -4V$ and it is biased to operate at $V_{GS} = -1.8V$.

$$g_m = -\frac{2I_{DSS}}{V_p}\left[1 - \frac{V_{GS}}{V_p}\right] = -\frac{2 \times 8m}{-4}\left[1 - \frac{(-1.8)}{-4}\right]$$

$$\boxed{g_m = 2.2\,mS}$$

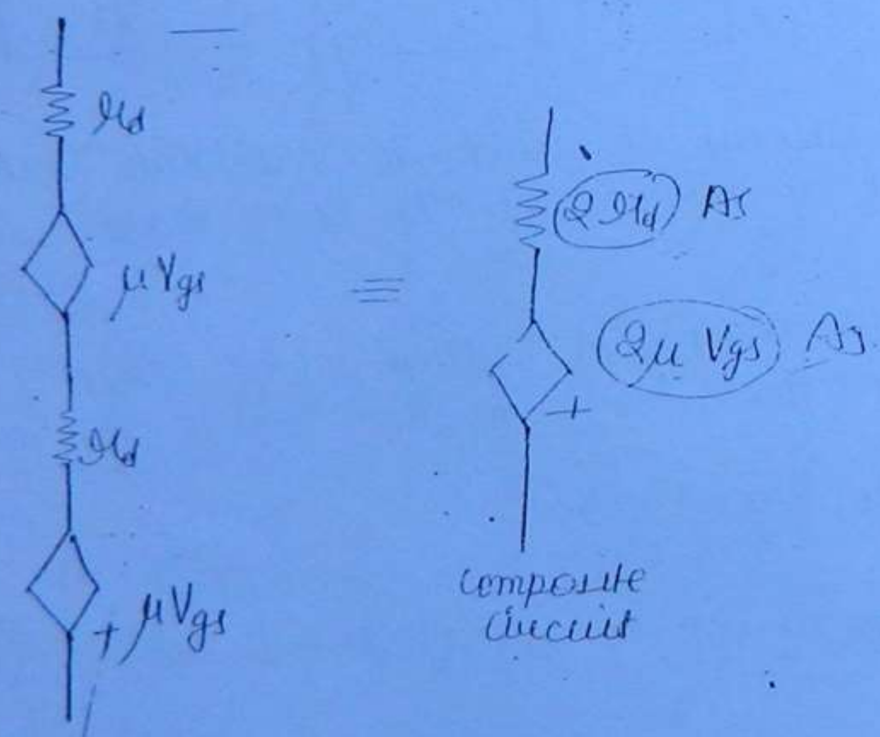
Prob When gate source voltage of FET changes from −3 V to −3.1 V and I_D changes from 1.3 mA to 1 mA assuming other parameters to be const. find g_m

soln

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = 3\ mS$$

Prob If two identical FET each having an amplification factor μ and drain resistance r_d are connected in series for composite circuit find its amplification and drain resistance

soln

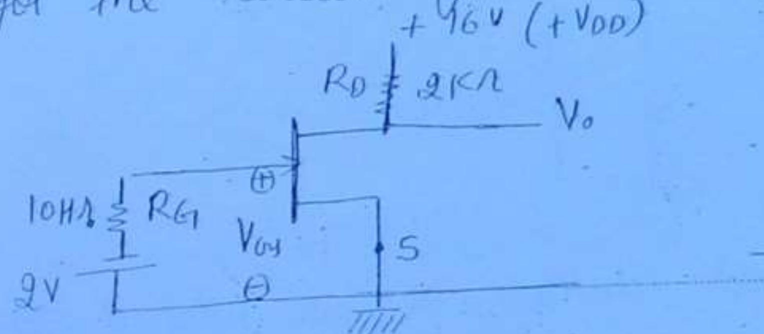


Prob If two identical FET each having a transconductance g_m and drain resistance r_d are connected in parallel for the composite circuit find there new values

Ans

$$\frac{r_d}{2} \text{ and } 2g_m$$

Prob For the circuit given below calculate V_{GS}, I_D & V_{DS}



FET data

$I_{DSS} = 10mA$

$V_P = -8V$

since $I_G = 0$

$$V_{GS} = -2V$$

$$\therefore I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

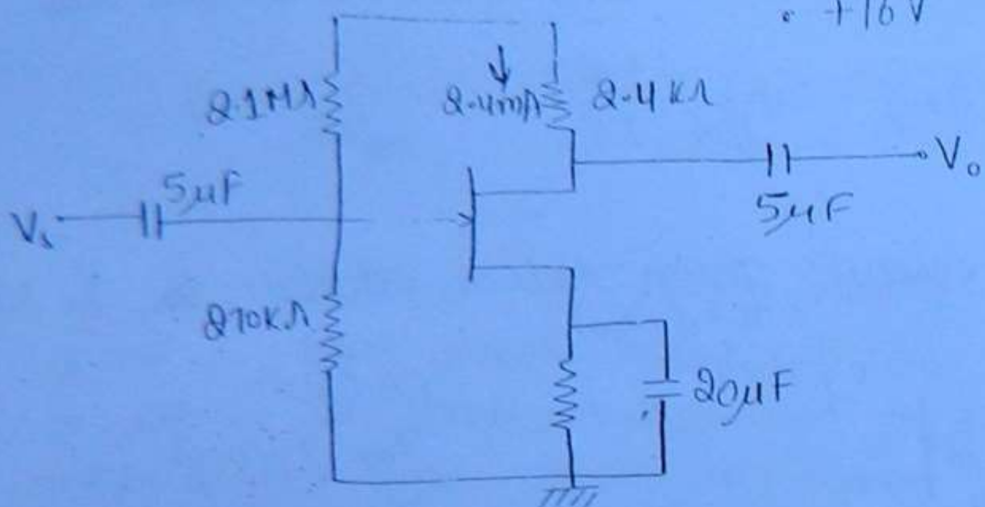
$$= 10\times10^{-3}\left[1 - \left[\frac{-2}{-8}\right]\right]^2 = 5.625mA$$

$$V_{DS} = V_o = V_{DD} - I_D R_D$$

$$= 16 - [5.625 \times 2k]$$

$$= 4.75V$$

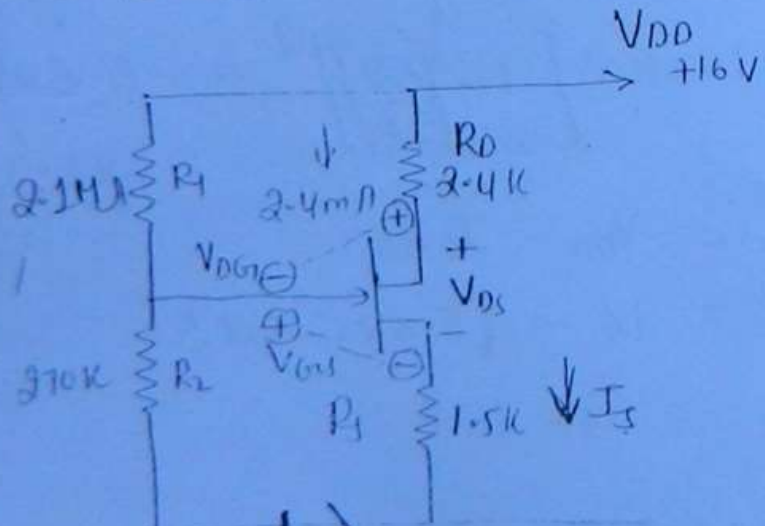
Prob Calculate V_{GS}, V_{DS} & V_{DG} :



→ It is a potential divider or self biased ckt.

V_s = signal voltage

→ Terminal voltages are calculated under DC analysis or under biasing condⁿ i.e. with zero i/p signal apply and therefore all capacitors in the ckt will be treated as OC.



→ By using approximate analysis i.e. By O.C. the gate

$$V_{R2} = \frac{V_{DD}\, R_2}{R_1 + R_2}$$

$$= \frac{16 \times 270K}{2.1M + 270K}$$

$$V_{R2} = 1.82 \text{ volt}$$

$$V_{R2} = V_{GS} + I_S R_S$$

$$1.82 = V_{GS} + 2.4\,m \times 1.5K$$

$$\Rightarrow \boxed{V_{GS} = -1.78\,V}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_{DS} = 16 - 2.4m\,[2.4K + 1.5K]$$

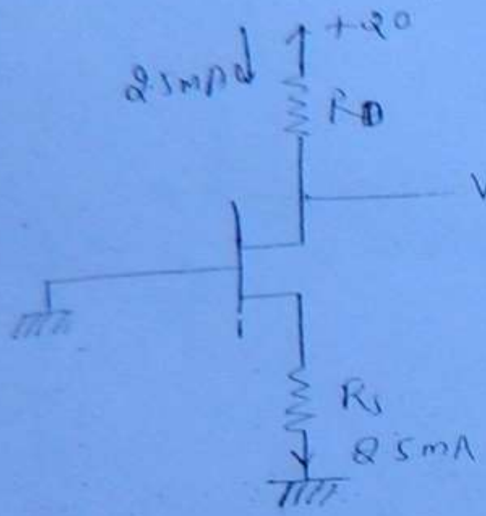
$$\boxed{V_{DS} = 6.64\,V} \text{ Ans}$$

$$V_{DS} = V_{DG} + V_{GS}$$

$$6.64 = V_{DG} + (-1.78)$$

$$\boxed{V_{DG} = 8.42\,V} \text{ Ans}$$

Qn: find R_D & R_S :→



$I_{DSS} = 6\,mA$

$V_P = -3\,V$

Soln —

$$R_D = \frac{(20-12)}{2.5} = \frac{80}{2.5 \times 10^{-3}} = \frac{80 \times 1000}{25}$$

$$= 3200\,\Omega = 3.2\,k\Omega$$

$$V_{GS} = V_P\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

$$V_{GS} = -1.06\,V$$

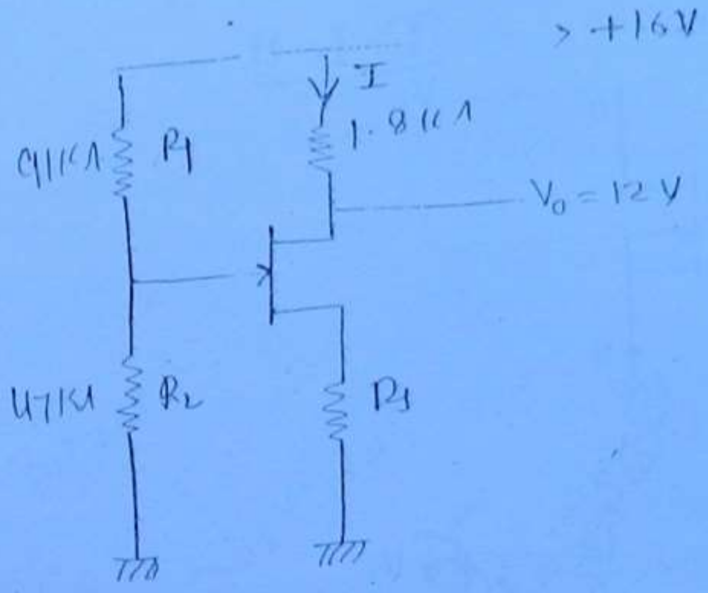
$$V_G = V_{GS} + I_S R_S$$

$$0 = -1.06 + (2.5m)(R_S)$$

$$\left|\frac{1.06}{2.5m}\right| = R_S$$

$$\boxed{R_S = 424\,\Omega}$$

Prob: If $V_{GS} = -2V$, find R_S



$$I = \frac{16-12}{1.8} = \frac{4}{1.8 \times 10^3}$$

$$I = 2.22\ mA$$

Soln

$$V_{R2} = \frac{47 \times 10^3 \times 16}{91+47}$$

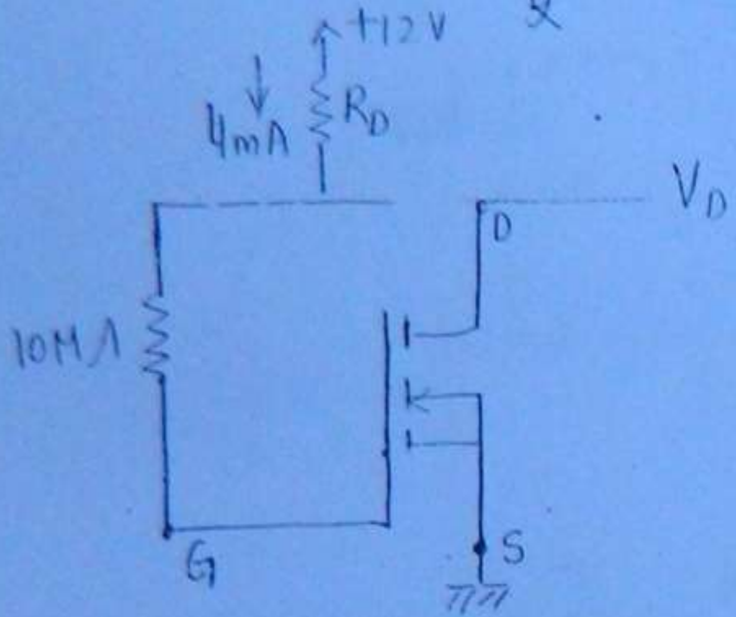
$$V_{R2} = \frac{47 \times 16 \times 10^3}{138 \times 10^3} = 5.44\ V.$$

$$V_G = V_{GS} + I_S R_S$$

$$5.44 = -2V + 2.22m\ (R_S)$$

$$\Rightarrow \boxed{R_S = 3.35\ k\Omega}$$

Prob Given that $V_D = \frac{V_{DD}}{2}$, find R_D ..



$$V_D = \frac{V_{DD}}{2} = \frac{12}{2} = 6\,V$$

$$R_D = \frac{12-6}{4m} = \boxed{1.5\,k\Omega}$$

END OF DAY

B · J · T ·

BIPOLAR JUNCTION TRANSISTER

BJT (Bipolar Junction transistor):-

Emitter	E	Highly doped	medium space
Base	B	lightly	smaller
Collector	C	med	largest

A bipolar device having both majority and minority carriers.

Invented by William Schokley (1947)
Barttain
Bardeen

Current Control device (CCD)

Low input res. device

when Compair to FET power Consumption is more.

Noisy device, due to the presence of minority Carrier.

Leakage Current are existing due to the presence of minority Carrier.

Temp. Sensitive device

* Emitter is highly doped to inject the majority Carrier into the base.

* Emitter is provided with medium area

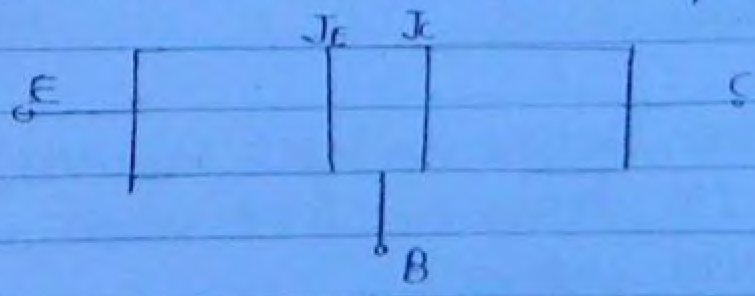
* Base is lightly doped to reduce the recombination.

* Transistor action take place in the base

* Base is provided with smallest area to reduce the transist time
  transist time – time taken by charge Carrier to move from E to C

* Collector is moderating doped

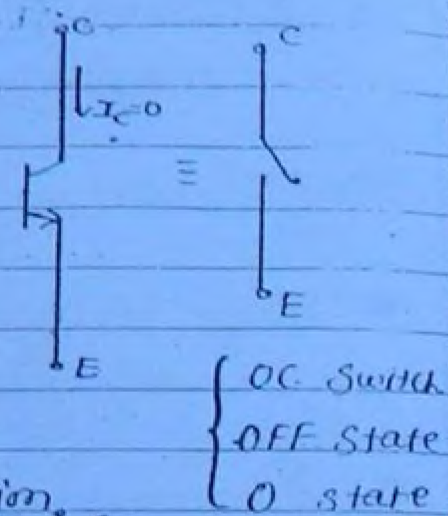
* Collector is provided with largest area to overcom heat dessipation.

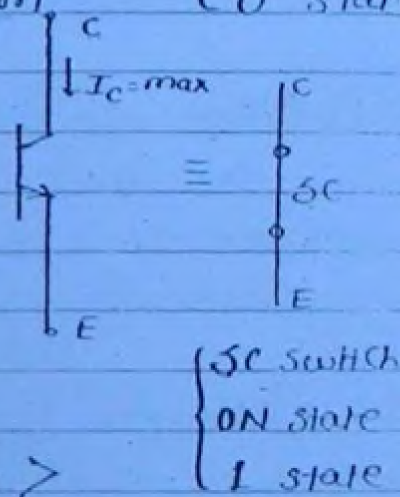


$J_E \rightarrow E \,\&\, B$

$J_C \rightarrow C \,\&\, B$

	J_E	J_C	
1.	RB	RB	Cutoff Region or OFF
2.	FB	FB	Saturation Region or (SAT)





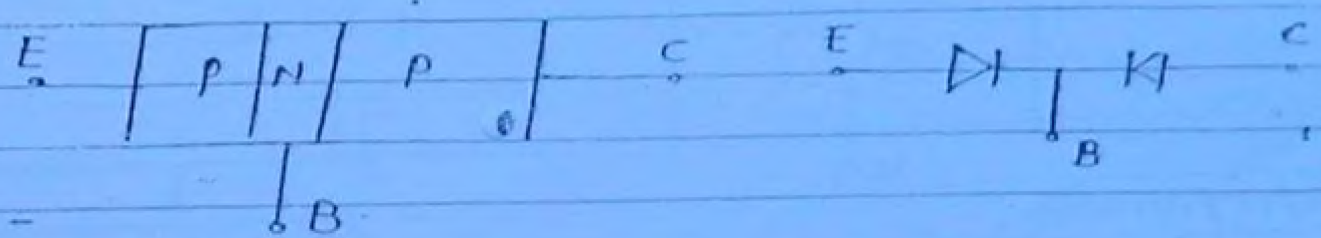
NOTE :- → If emitter junction voltage > Collector Junction voltage the transistor is under forward saturation region

→ If Collector Juction voltage > emitter Junction Voltage the transistor is in under reverse Saturation region.

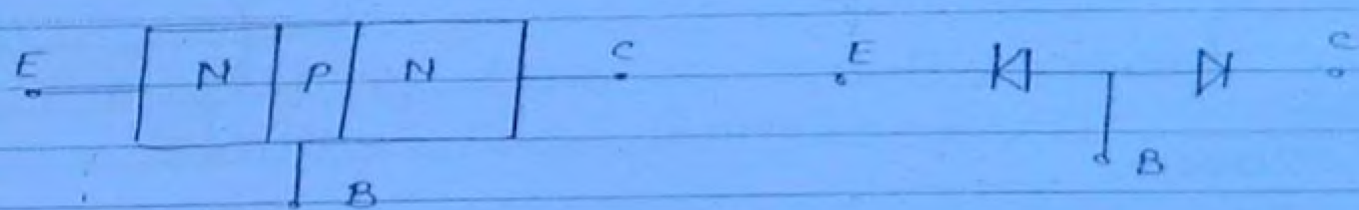
3.	FB	RB	Active Region (forward active Region) (Working as amplifier)
4.	RB	FB	gain is negligible (never operation in this region)

Diode equivalent circuit of BJT :-

PNP transistor :-



NPN transistor :-



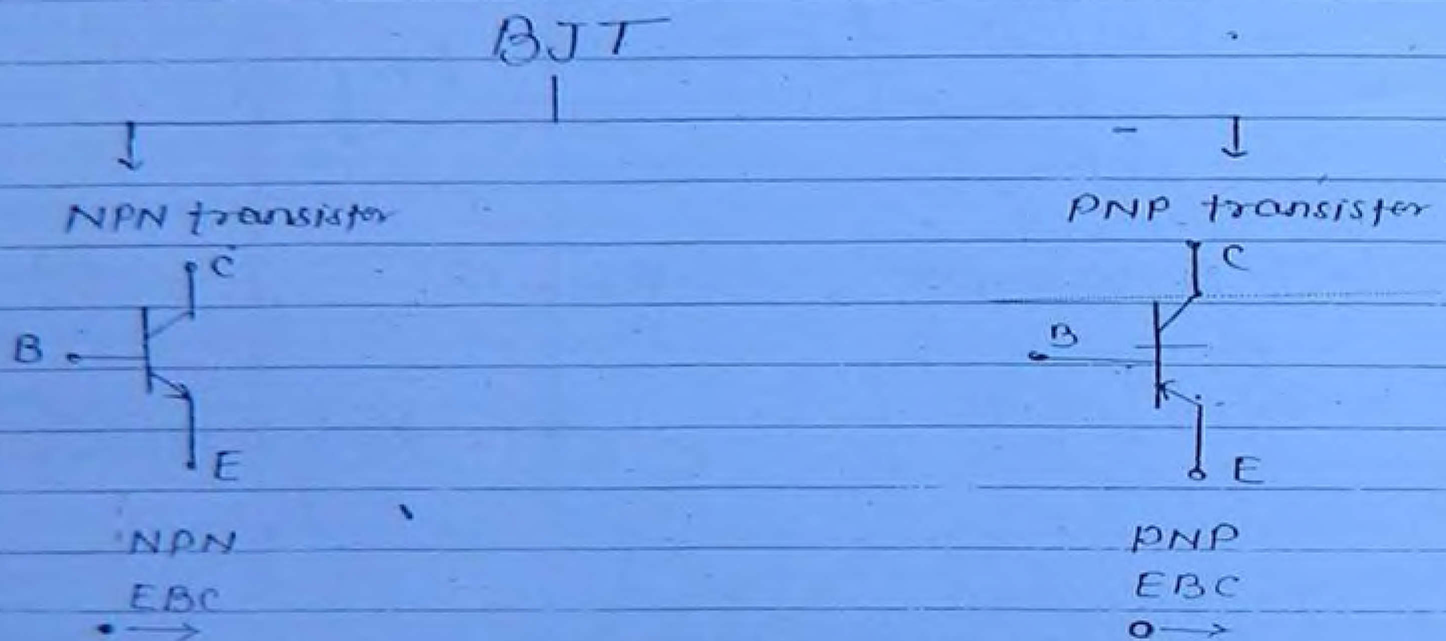
* A BJT can be represented by two diodes are connected back to back.

* When two diodes are connected as shown in the equivalent ckt, it will not work as a BJT because.

i> There is no bonding force in betⁿ the two diodes

ii> The base width will become very large so that no charge carrier will be reaching the collector.

NOTE - The transistor can work as a switch when operated both in the Cutoff and Saturation Region.



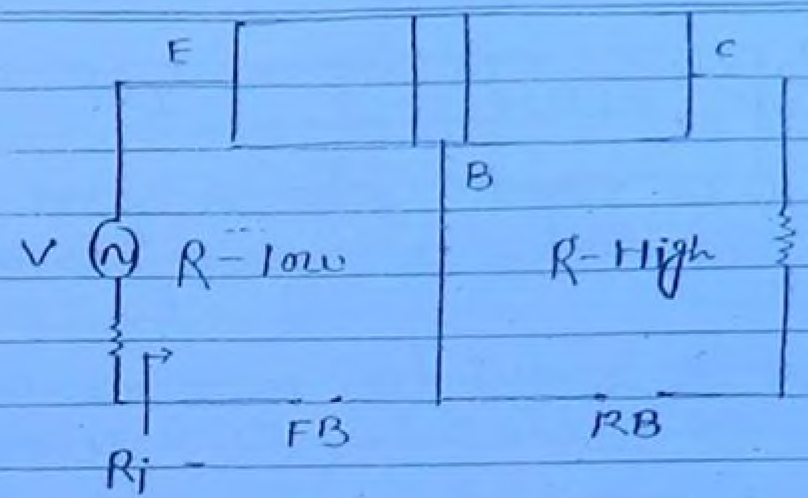
* In NPN transistor current is predominantly (mainly) by the flow of e^-

* In PNP transistor Current is mainly due to both

* NPN transistor is superior to PNP transistor because $\mu_n > \mu_p$

Q. In a transistor, arranging the doping level of E, B, C in acending order to the current sequence is B, C, E

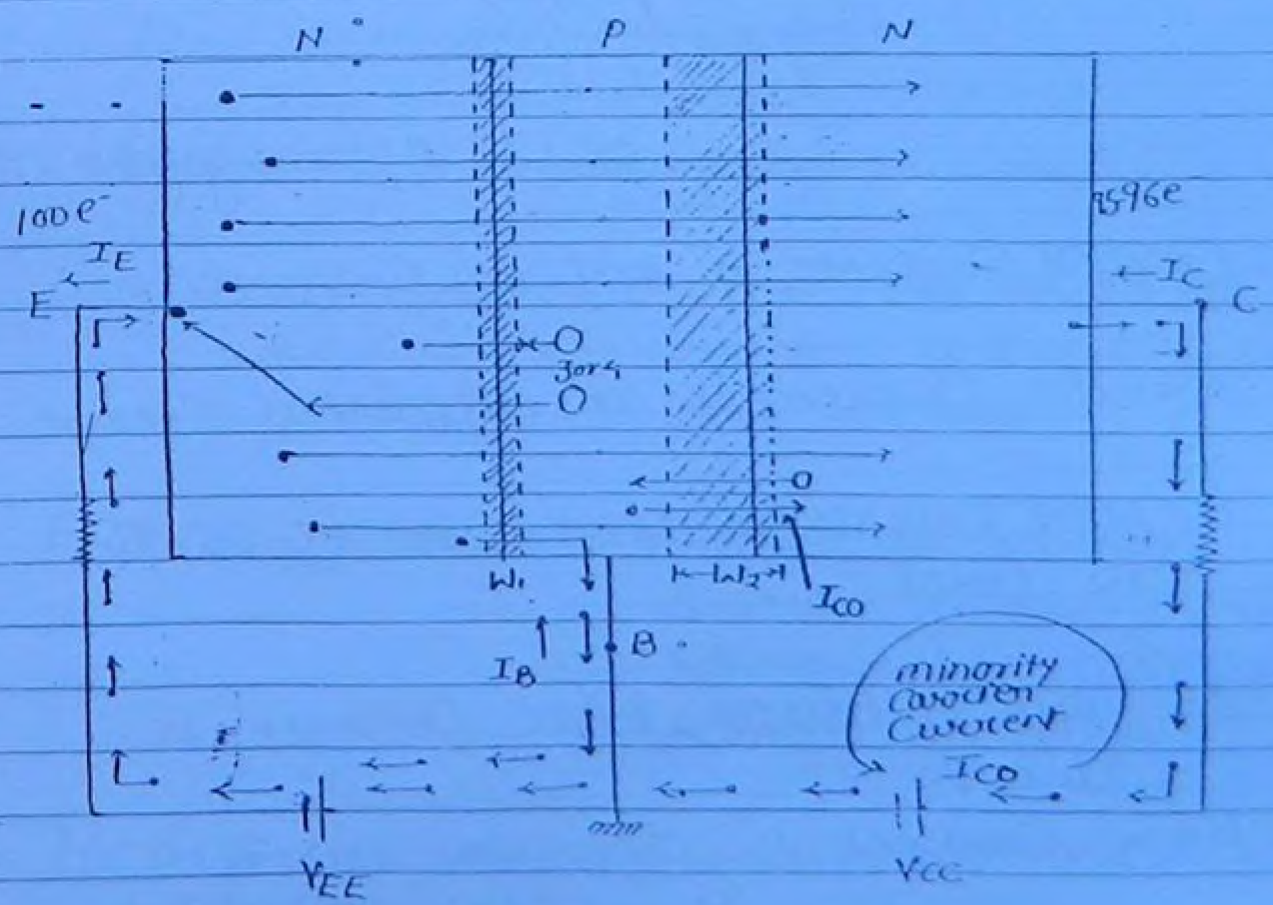
Q In the transistor arranging the physical dimension of E, B, C in the decending order or decreasing order the current sq. is C, E, B

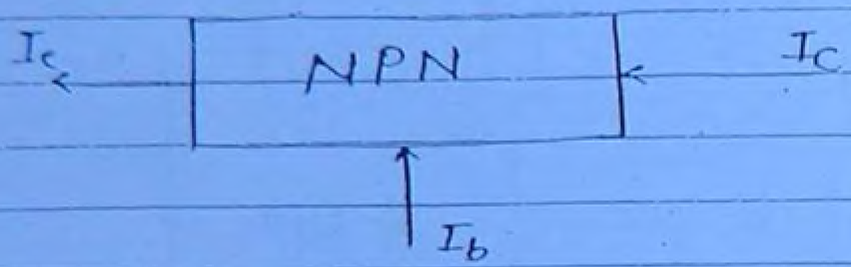


TRANSFER + RESISTOR = TRANSISTOR

In BJT input res. is small because emitter base junction is FB

Operation of NPN transistor under active Region



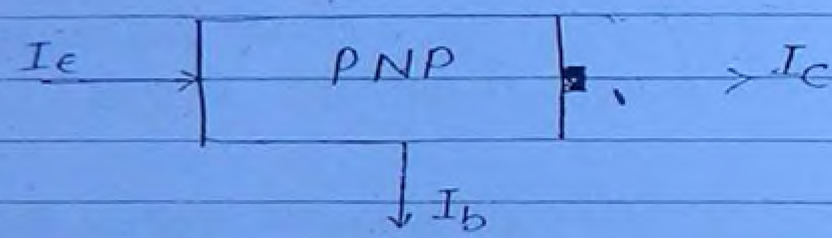


$$-I_e = I_c + I_b$$

$$I_e = I_c + I_b \text{ in magnitude}$$

I_b is very small, negligible (μA)

$$\boxed{I \approx I_e}$$



$$I_e = -I_c + I_b$$

$$I_e = I_c + I_b$$

$$\boxed{I_c \approx |I_e|}$$ After negligible I_b

* Emitter Current is majority Current.
* Emitter Current is a diffusion Current.
* In NPN transistor, base Current is due to holes.
* In PNP transistor, base Current is due to e^-
* Base Current is diffusion Current.

* Base Current is a recombination Current.

* In NPN Tr base Current is due to the no holes getting recombine with the incoming e⁻.

* Recombination Current force only in BJT

* Tr action take place in the base region.

* The movement or flow of charge Carrier betn base and collector in the Tr is due to diffusion of minority Carrier.

* Collector Current is a diffusion Current

* Ico is a drift Current.

* Collector is made up of two Components.

i) majority Current → It is due to 95-96 emitter electrons reaching the Collector

ii) Minority Current → It is the minority Carrier Current in the RB Collector Junction. becouse of temp.

* In a Tr all the major Currents are diffusion Currents.

In a Tr there are three currents components
i) diffusion current
ii) drift current
iii) recombination current

? In a Tr recombination under
a only into the emitter
b in the emitter and base
c only in the base
✓d In emitter base and collector Jn.

Ico :-
Collector reverse saturation current.
or Collector leakage current
or minority carrier current
or thermaly generated current

	Ge Tr	Si Tr
I_{CO}	μA	mA

* Ico is highly sensitive to temp.
* Ico is double for every 10°C
* for 1°C Ico approx increases by 7%
* Ico is independent of collector junction voltage
* Ico is a drift current.

$$I_{CO(T_2)} = I_{CO(T_1)} \left[2^{\frac{T_2 - T_1}{10}} \right]$$

General eqⁿ for Collector Current (I_C) :-

In the active region of Tr

$$I_C = \beta I_b + (1+\beta) I_{CO}$$

↓ majority Carrier Current

↓ minority Carrier Current

$$I_C \approx \beta I_b$$

Base width of a Tr :-

* In a Tr always the base width must be less than diffusion length of the Charge Carrier (minority Carrier moving from base to Collector)

$$W_B < L$$

In the NPN Tr

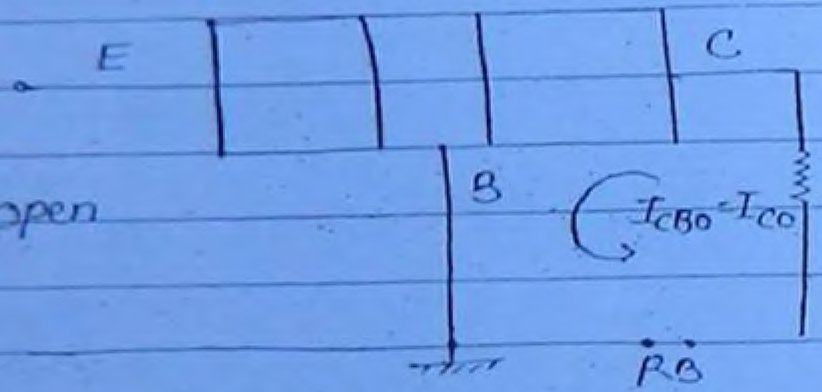
$$W_B < L_n$$

$$W_B < \sqrt{D_n \tau_n}$$

* If the above Condition is satisfy the Tr action will take place in the transistor.

ICBO :-

It is the leakage current passing from collector to base with a emitter open circuited.



$I_{CBO} = I_{CO}$ Collector reverse saturation current.

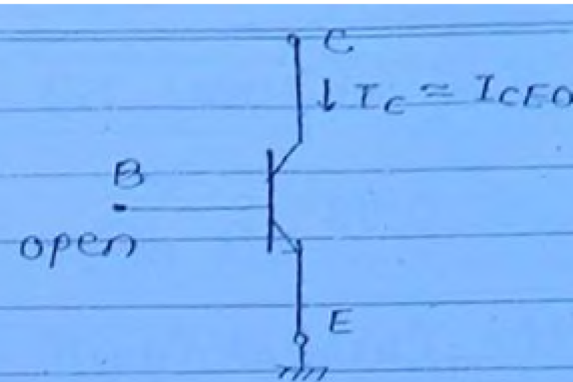
* I_{CBO} is also called emitter cutoff current.

ICEO :-

It is the leakage current passing from collector to emitter with base open cked.

Also called base cutoff current

If a Tr working under active region and if base terminal is suddenely open. The current in the Tr is I_{CEO}



$I_C = \beta I_b + (1+\beta) I_{CO}$

or

$= \beta I_b + (1+\beta) I_{CBO}$

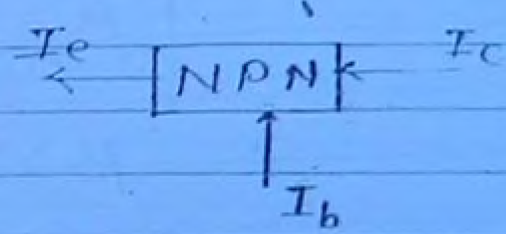
Since $I_b = 0$

$I_C \approx I_{CEO}$

Imp

$$\boxed{I_{CEO} = (1+\beta) I_{CBO}}$$

Alpha (α) of the Tr :-



$$\alpha = -\frac{I_c}{I_e}$$

Since I_c & I_e have opp. sign

α is +ve

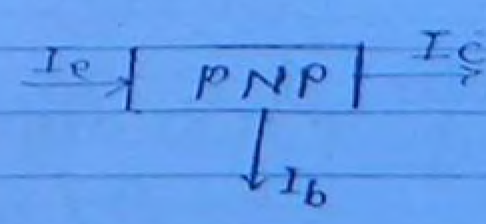
$$\boxed{\alpha = \left| -\frac{I_c}{I_e} \right|}$$

[∵ emitter current is slightly greater than collector current.

$\alpha \approx 1$

α is slightly < 1

Typical value = 0.98



* Max Value of $\alpha = 1$ (ideal Tr)
* Practical Tr $\alpha = 0.98$

* α is called the current gain of Common base Tr

$$\Rightarrow \boxed{\alpha = \frac{\beta}{\beta+1}}$$

Beta [β] of the Tr :-

$$\boxed{\beta = \frac{I_C}{I_b}}$$

- $\beta >> 1$
- Typ. = 49

β in terms of α is :-

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

* β is the most important specification of the Tr
* In Ge Tr β doubles for every 50°C
* In Si Tr β doubles for every 75°C

$\beta \uparrow$ with temp

* β is the current gain of Common emitter

β

β or β_{dc} or h_{FE} $= \frac{I_c}{I_b}$

β or β_{ac} or h_{fe} $= \frac{\partial I_c}{\partial I_b} = \frac{\Delta I_c}{\Delta I_b}$

$\beta_{dc} > \beta_{ac}$

or $h_{FE} > h_{fe}$

Gamma (γ) of the Tr :-

$$\gamma = \frac{-I_e}{I_b}$$

Since I_e & I_b have opp sign; γ is

$$\boxed{\gamma = \left|\frac{I_e}{I_b}\right|}$$

$$\boxed{\gamma = \beta + 1}$$

⇒ Typical value - 50

* γ is for the current gain of common Collector Tr (CC Tr)

Relationship between α, β, γ of the Tr

$$\gamma = 1 + \beta = \frac{1}{1-\alpha}$$

In a Tr various current gain are α, β, γ and arrangin in the acending order in the seq of α, β, γ.

Emitter Current in terms of base current:-

$$I_e = I_c + I_b$$

but $I_c \approx \beta I_b$

$$\boxed{I_e \approx (1+\beta) I_b}$$

or

$$\boxed{I_e \approx \frac{I_b}{1-\alpha}}$$

Effect of temp on Collector Current (I_c):-

$$I_c = \beta I_b + (1+\beta) I_{co}$$

As $T\uparrow$, $I_{co}\uparrow$

& $\beta\uparrow$

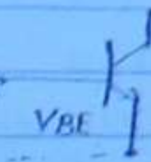
$$\boxed{I_c\uparrow \text{ with } T}$$

PSU

* Collector ~~Colle~~ Current increases with temp. BJT has +ve temp. Coefficient (PTC)

Standard eqn for I_E:

$$I_E \approx I_{CO} e^{V_{BE}/nV_T}$$



$$\left[\because I_f \approx I_o e^{V_f/nV_T}\right]$$

In a Tr emitter current is the forward current of emitter diode.

Base emitter voltage of the Tr:-

$$V_{BE} < 1V$$

for Ge Tr $V_{BE} = 0.1V$ to $0.5V$ typ $0.2V$
for Si Tr $V_{BE} = 0.6V$ to $0.9V$ typ $0.7V$

$$\left[\downarrow V_{BE} \approx nV_T \downarrow \log\left(\frac{I_C}{I_{CO}\uparrow}\right)\right]$$

$\therefore V_{BE} \downarrow$ with T

IMP

for $1°c$ $V_{BE} \downarrow$ by $2.3mV$

At room temp

In NPN Tr

	Ge Tr	Si Tr
V_{BE} (cutin)	0.1V	0.6V
V_{BE} (Active)	0.2V	0.7V
V_{BE} (Sat)	0.3V	0.8V

Drift Tr and diffusion Tr :-

In a diffusion Tr base current is made only with diffusion current.

A normal Tr is a diffusion Tr.

In a drift Tr base current is made of both drift current & diffusion current.

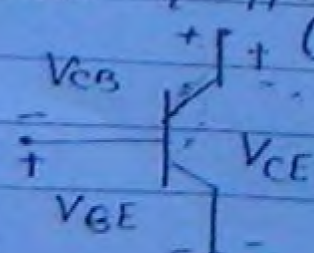
Recombination Agent :-

The best recombination agent is hole.

Recombination agent use to increase the recombination in the base region.

In a special Tr a small quantity of hole is introduced into the base region. They will formed in local center. They will be working as TRAP the e^-. so that the recombination will be increases in the base region.

Terminal Voltage of Tr :-

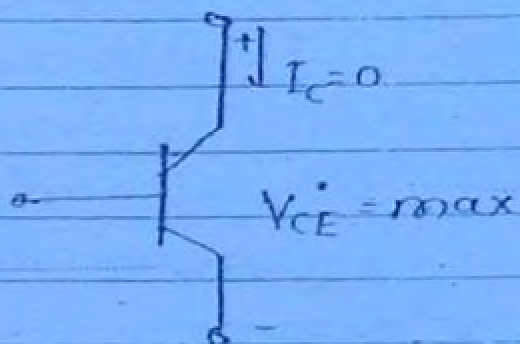


$$V_{CE} = V_{CB} + V_{BE}$$

Power dessipation of a Tr (P_T):-

$$P_T = |I_C| V_{CE} \text{ watts}$$

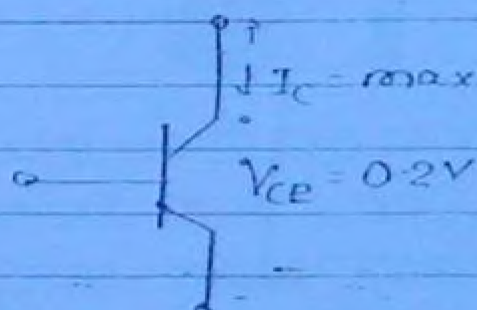
In the cutoff region:-



$P_T = 0$

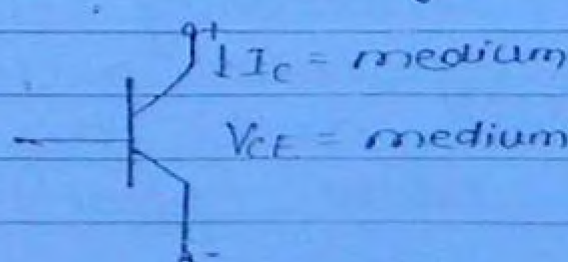
In Cutoff region the tr Cannot Consume power.

In the Saturation Region:-



P_T = negligible

In the active Region:-



P_T = large

* The tr will Consuming max power when operated in the active region.
* The tr cannot Consume any power when operated in cutoff region.

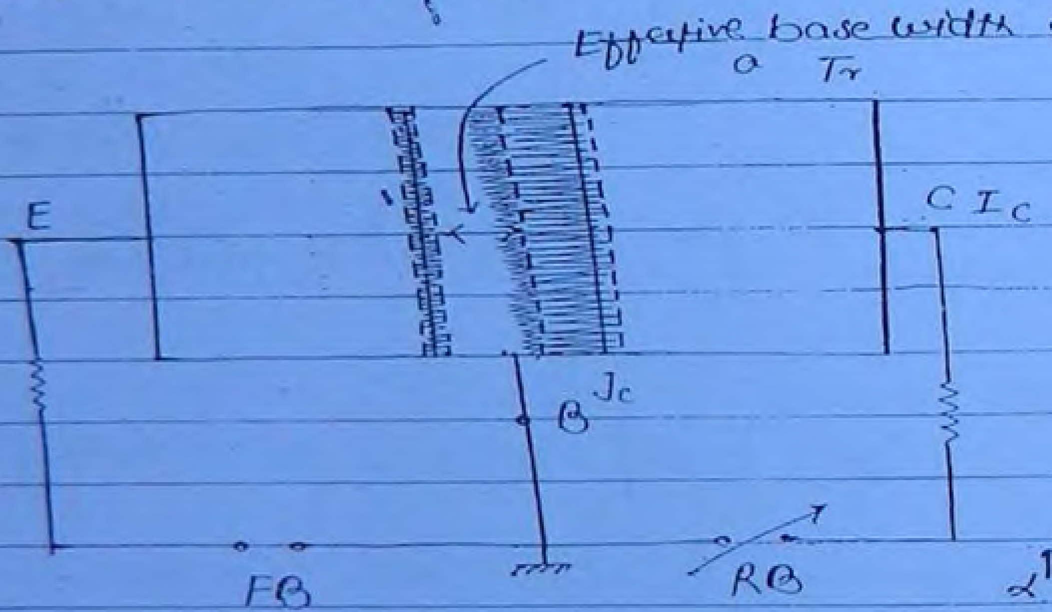
IMP

Base Width Modulation :-

(small change
or small variation)

Also Called "EARLY Effect"

* The process where the effective base width of the transistor is altered by changing the Collector junction is called base width modulation.



$\alpha\uparrow = \frac{I_C\uparrow}{I_E}$

$\beta\uparrow = \frac{I_C}{I_b\downarrow}$

* In a Tr by increasing Collector junction voltage, base width of the Tr is reduce and this property is called early effect.

* If Collector to base jn (C-B Jn) is more RB the base width of the Tr reduce.

4

* Base Narrowing = early effect

* Due to the early effect.

i> The chances of recombination in the base is reduce so that more charge carriers will be reaching the collector and therefore I_C increase.

ii> α is slightly increases (0.9 to 0.99)

iii> β increases by larger value.

iv> Transist time is reduce.

* The effective base width of the Tr will offer a res. $r_{bb'}$ called base spread res. to the flow of signal current at high freq. and this res. will reduce the performance of device.

* At low freq. the effect of $r_{bb'}$ is neglected.

* The process where the effective base width of the Tr is reduce to 0 by applying larger collector junction voltage is called punch through or Reach through.

Breakdown Voltage of Tr :-
(V_{Br}) or (B_V)

$$V_{Br} \propto \frac{1}{\text{doping}}$$

In a Tr collector junction break down voltage is always greater than emitter junction breakdown voltage.

$$\boxed{B_{V\,C-B} > B_{V\,C-B}}$$

In a Tr emitter junction breakdown is due to zener effect and collector junction breakdown is due to avalanche effect.

Problems:-

Q. A Tr has $\alpha = 0.98$ $\beta = ?$

$$\beta = \frac{\alpha}{1-\alpha}$$

$$= \frac{0.98}{1-0.98}$$

$$\boxed{\beta = 49}$$

Q. A Tr has $\alpha = 0.99$ $\beta = ?$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = 99$$

$\therefore$ $\alpha = 0.98$ to 0.99 small variation
$\beta = 49$ to 99 large variation.

Q. A Tr having $\beta = 49$

$I_b = 5\mu A$

$I_e = (1+\beta) I_b$

$= (1+49)\, 5\times10^{-6}$

$= 250\mu A$

$I_e = 0.25 mA$

Q. A Tr has $\beta = 59$.

$I_b = 10\mu A$

$I_{CO} = 10 nA$

$I_C = ?$

$I_C = \beta I_b + (1+\beta) I_{CO}$

$= 59\times10\times10^{-6} + (1+59)\, 10\times10^{-9}$

$I_C = 590.6\mu A$

Q. A Tr has $I_e = -10 mA$

$I_c = 9.95 mA$

find I_b, α, & β

$I_e = I_c + I_b$ in magnitude

$I_b = I_e - I_c$

$= 10mA - 9.95mA$

$= 0.05mA$

$I_b = 50\mu A$

$\beta = \frac{I_c}{I_b}$

$= \frac{9.95mA}{0.05mA}$

$\beta = 199$

$$\alpha = \frac{\beta}{\beta+1} = \frac{199}{200} = 0.995$$

Ans.

Q. A Tr has a leakage current of 5 µA when emitter is OC. If base is OC the leakage current are 200 µA find α & β of the Tr.

Sol.

$$I_{CBO} = 5\,\mu A$$

$$I_{CEO} = 200\,\mu A$$

$$I_{CEO} = (1+\beta)\, I_{CBO}$$

$$1+\beta = \frac{I_{CEO}}{I_{CBO}} = 40$$

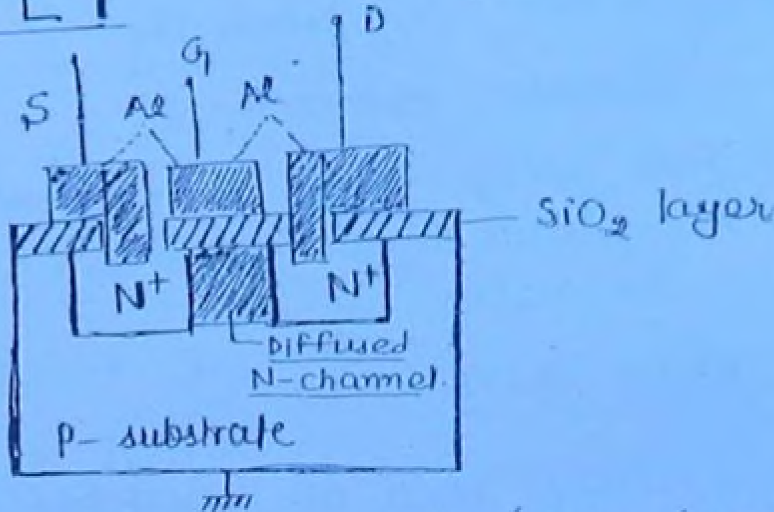
$$\boxed{\beta = 39}$$ Ans.

$$\alpha = \frac{\beta}{\beta+1}$$

$$= \frac{39}{40}$$

$$\boxed{\alpha = 0.975}$$ Ans

MOSFET



N- channel MOSFET. (Depletion)

→ An Integrated circuit or semiconductor chip
→ Fabricated by VLSI by using planar technology.
→ The thickness of Si wafer is 0.5 µm
→ For N channel MOSFET substrate is p-type
→ For P channel MOSFET substrate is N-type
→ The thickness of SiO_2 is 1000 Å to 2000 Å.
→ The larger input resistance of MOSFET is due to SiO_2 layer.
→ Voltage control device
→ Symmetrical device
→ A capacitance (parallel) is formed at the gate section with Al plate and SC channel as the two plate of capacitor and SiO_2 as the dielectric material
→ MOSFET is a capacitor
→ MOSFET is voltage control capacitor (VCC)
→ Channel is also called inversion layer
→ Entire area of MOSFET is less then 5% of area required for BJT.

when compared to JFET MOSFET is smaller in size and easier to fabricate

JFET is a discrete component.

MOSFET is less noisy then compared to JFET it is due to grounding the substrate So that it will filter the noise

→ MOSFET is faster then JFET

→ MOSFET are widely used as switched in digital circuits.

→ MOSFET is very sensitive static electrical noise. and static electrical disturbance.

→ In the Depletion MOSFET there will be a preexisting channel

→ In the Depletion MOSFET the channel is diffused channel

→ In BJT is a discrete component

→ In BJT there will be a minority carrier storage time

→ In MOSFET minority carrier storage time is zero

→ (due to absence of minority carrier).

→ In MOSFET turn-off time is very small typ value 75ns

→ When compared to BJT MOSFET is relatively more suitable for high frequency application and this is due to absence of minority carrier storage time.

→ BJT is faster then MOSFET

Depletion Mode :→

max $I_D \rightarrow I_{DSS}$

$\Rightarrow$ * $\boxed{I_D \leq I_{DSS}}$

Enhancement mode :→

min $I_D \rightarrow I_{DSS}$

$\Rightarrow$ * $\boxed{I_D \geq I_{DSS}}$

→ JFET is always operated under depletion mode.

→ * N- channel depletion MOSFET is sometimes called dual MOSFET becoz it is suitable to operate both in the depletion mode and enhancement mode.

→ P- channel depletion MOSFET is more popular for enhancement operation

→ N-mos is faster than p-mos (becoz $\mu_n > \mu_p$)

→ Pmos is easier to fabricate.

→ Pmos is bulky.

→ Nmos suffer from ion contamination problem during the fabrication

→ To get equal performance between n mos and pmos pmos require twice the area require for n-mos

→ The main advantage of nmos is higher package density (it can store more information in the smaller area)

CMOS.

- CMOS consist of pmos and nmos.
- Input resistance R_i $10^{15}\Omega$.
- It will not consume any power or power dissipation is zero.
- → Major application as a Inverter (NOT gate).
- → In the cmos Inverter, whatever the i/p signal apply one transistor is ON and other is OFF

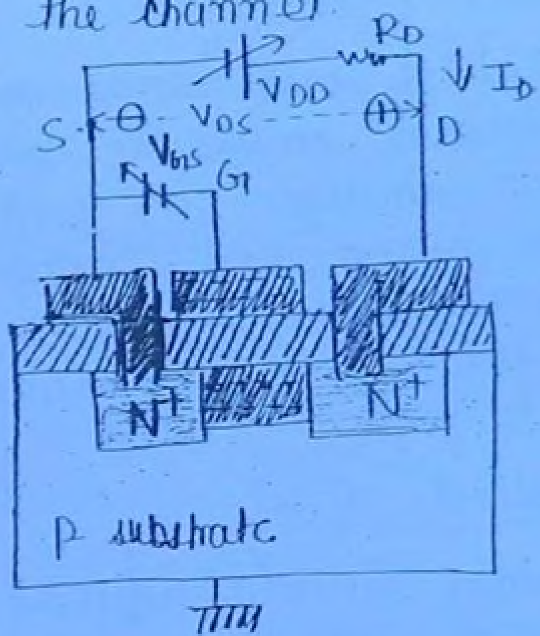
* VMOS.

⇒ Vertically grooved MOSFET.
→ It is a asymmetrical MOSFET
→ Voltage controlled Device.
→ VMOS is a power MOSFET (it can handle large amount of power when compare to normal MOSFET)
→ Vmos is faster then normal MOSFET
→ Response time is very small (Typ value 75ns).

(only for conventional ckt's)

4 **Operation of N-channel Depletion MOSFET in Depletion mode**

→ The principle of Depletion mode the applied gate to source voltage must reduce the majority carrier of the channel.



~~Operation of N-channel Depletion MOSFET~~

→ if $V_{GS} = 0$

⇒ max I_D → I_{DSS}

if V_{GS} is applied

−2V	$I_D \downarrow$
−4V	$I_D \downarrow$
−6V	$I_D \downarrow$
−8V	$I_D = 0$

⇒ For N-channel MOSFET Drain is positively biased with respect to source and to operate under depletion mode the gate is −vely biased w.r.t source

→ In n-channel depletion MOSFET :→

1. channel potential increases from S to D.
2. Inversion charge increases from S to D.

→ If V_{GS} is kept '0' ($V_{GS}=0$) :→

The gate is provided with zero voltage and therefore the inversion charge is zero and the maximum negative charges (e^-) will be moving from source to drain and therefore the drain current is maximum and is given by I_{DSS} (Drain to source safe current or saturation current)

→ When V_{GS} is applied

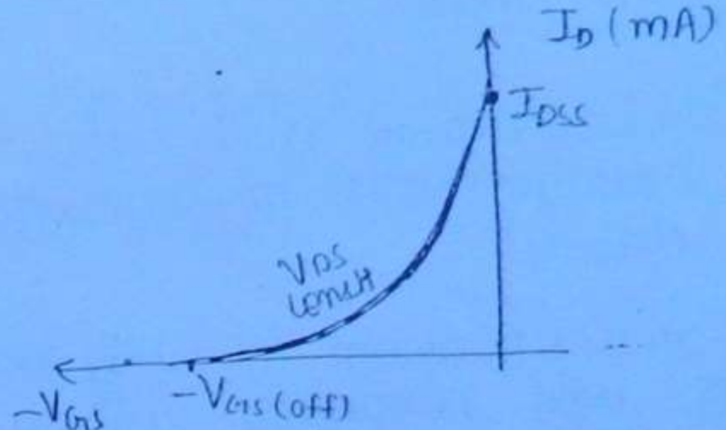
The gate is provided with a negative voltage and therefore +ve charges are created in the channel and due to the recombinations less negative charges will be reaching the drain and drain current is reduced

I_D further decreases as gate is given with more negative voltage.

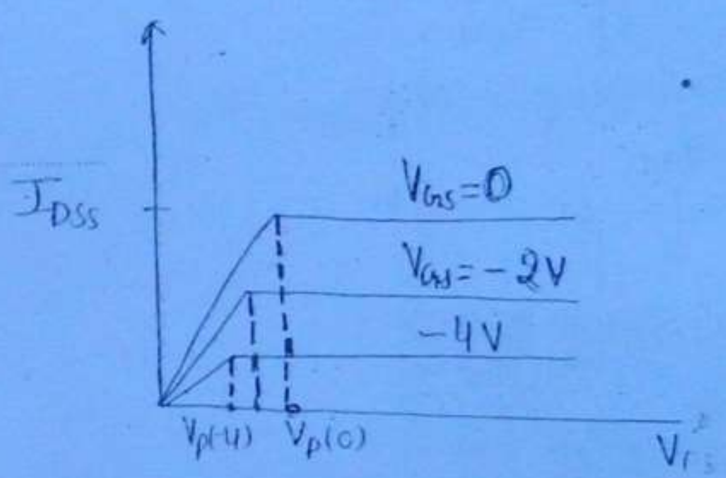
When gate is given sufficiently more negative voltage, a large no of +ve charges will be created in the channel and they will result a total recombination so that no negative charges will be reaching the drain and I_D reduces to zero ($I_D = 0$) Now channel is cut-off.

→ The transfer and drain characteristic for N-channel Depletion MOSFET under depletion mode

Transfer characteristics :→



Drain characteristics



→ The equation for drain current in depletion mode is

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \text{ Amp}$$

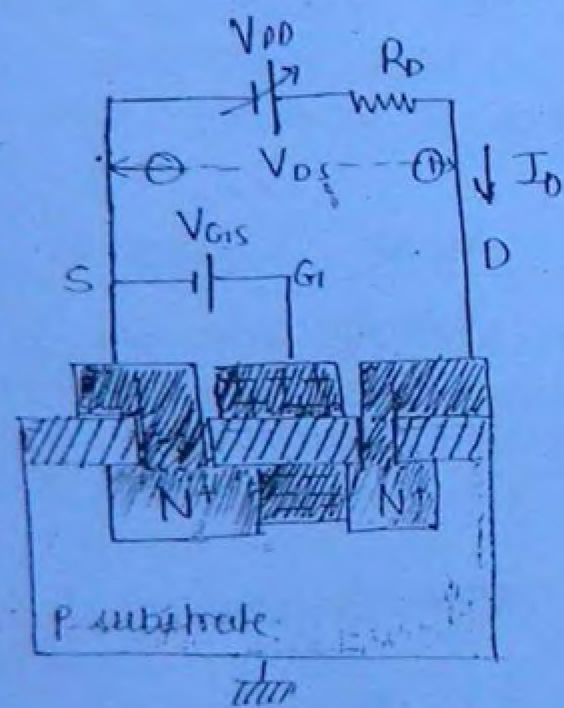
→ The polarity of V_{GS} and V_P are same.

→ The above equation indicate in depletion MOSFET under depletion mode, the drain current decreases as a parabolic variation with V_{GS}.

Operation of N-channel Depletion MOSFET under enhancement mode.

→ The principle of enhancement mode is the applied gate to source voltage must increase the majority carriers of the channel.

→ For N-channel MOSFET drain is +vely biased w.r.t the source and to operate under enhancement mode gate is +vely biased w.r.t source.



→ **When $V_{GS} = 0$:→**

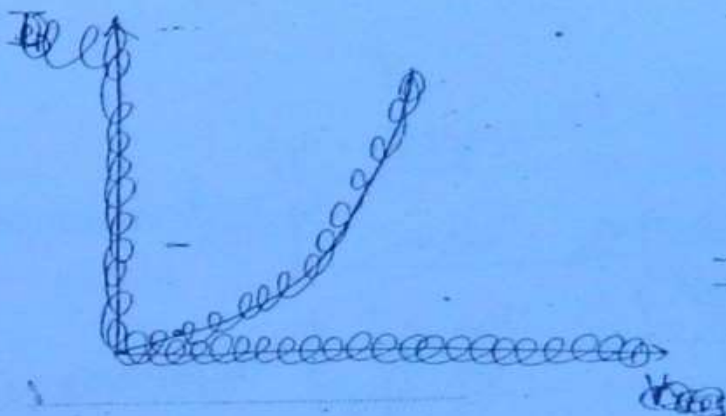
The gate voltage is zero and therefore inversion charge is zero and therefore minimum no. of -ve charges will be moving from source to drain & drain current is minimum and is denoted by I_{DSS} (drain to source sat current).

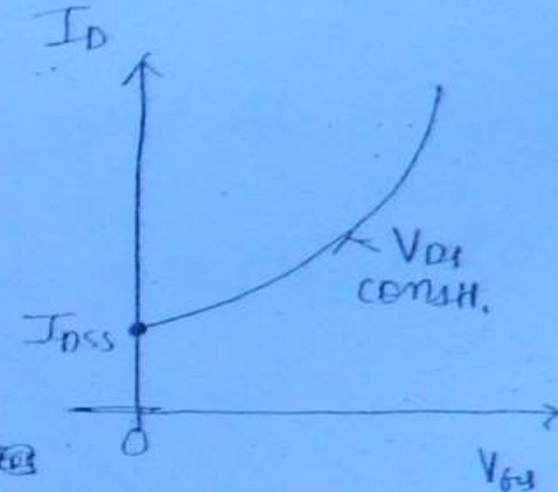
→ **When V_{GS} is applied.**

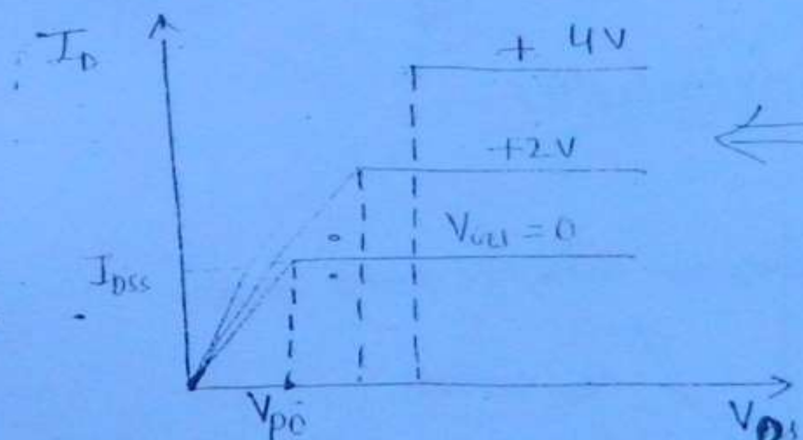
The gate is provided with a +ve voltage and therefore -ve charges are created in the channel and this will increase no. of -ve charges to drain & I_D increases & is greater than I_{DSS}.

: I_D further increases if gate is given small +ve voltage

- Transfer characteristics & drain characteristics for N-channel depletion MOSFET under enhancement mode.







⇐ Constant current characteristics

→ V_{PO} is the minimum pinch-off voltage

→ MOSFET is now working under pinch-off mode

→ Under pinch-off condⁿ :-

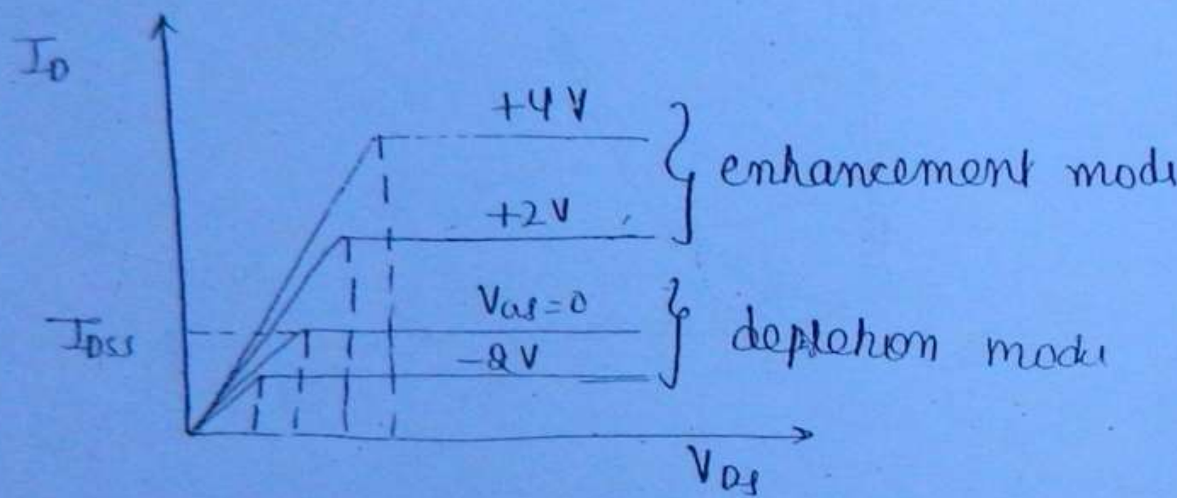
$$\Rightarrow \boxed{\min V_{DS} = V_{GS} + V_P}$$

$$\boxed{I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2}$$

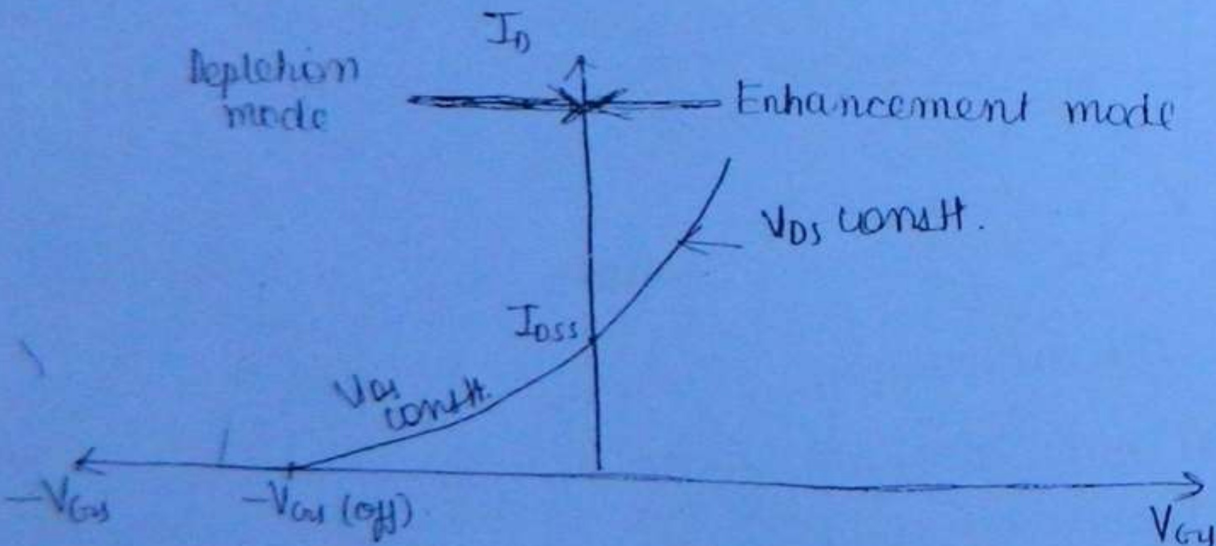
V_{GS} & V_P must have opposite sign.

→ The eqn for I_D indicates that I_D increases as a parabolic variation with V_{GS}.

Characteristics curve for N-channel depletion MOSFET.



Drain Characteristics



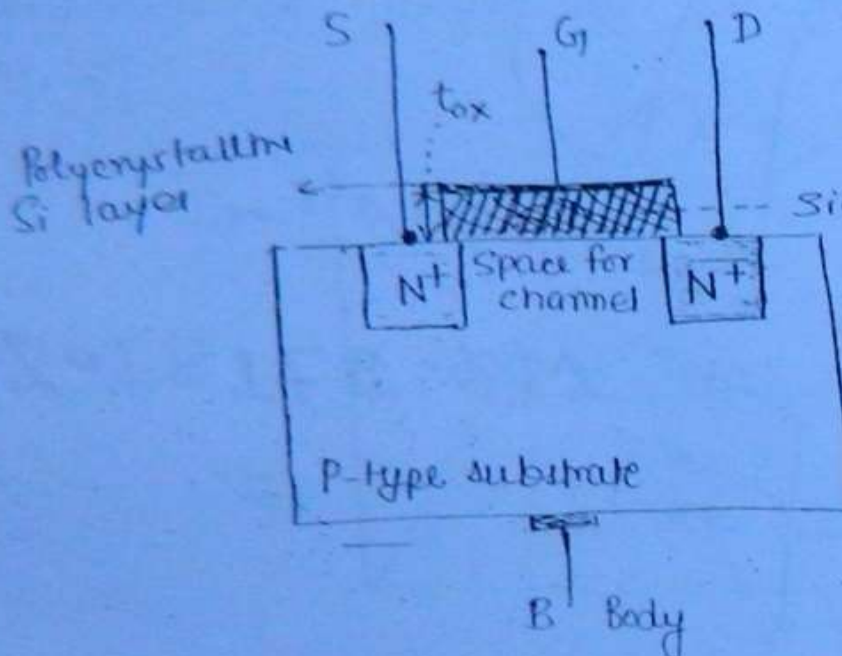
→ In the depletion MOSFET channel is diffused channel

→ In de MOSFET if V_{GS} is kept zero then $I_D = I_{DSS}$.

Enhancement MOSFET :-

or

E- only MOSFET



$t_{ox} \rightarrow$ Oxide Thickness.

→ E- only MOSFET is a modern MOSFET in which the Al plate are replaced with polycrystalline Si material.

→ E- only MOSFET is smaller in size, economical and also provide better performance then Depletion MOSFET

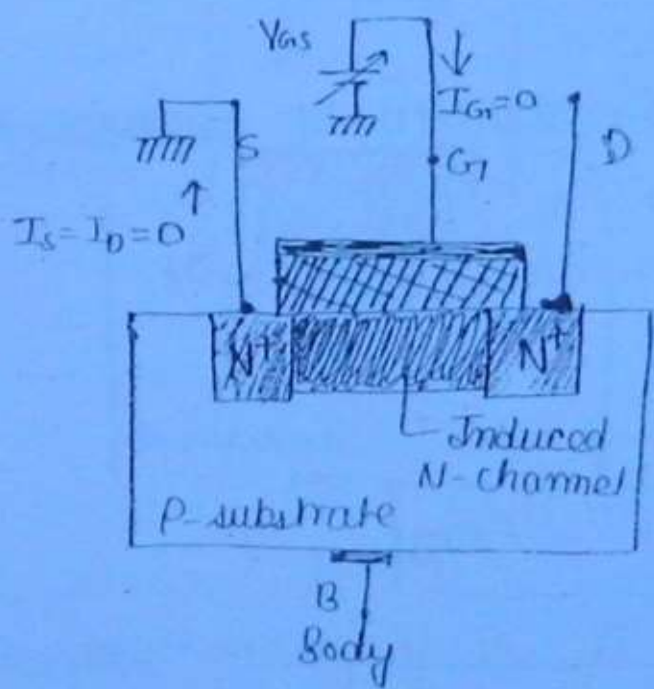
→ In E- only MOSFET the source and drain will be kept apart so that there is no channel / existing in between source and drain regions

→ In E- only MOSFET there is no prexisting channel and the channel has to be created by applying proper gate to source voltage

When proper gate to source voltage is applied and then body is grounded the gate to source voltage is also appearing between gate and body of MOSFET. Due to electric field intensity produced channel is induced in between the two N^+ region

In the E-only MOSFET the channel is induced channel.

The channel is a flat channel of length 'L' as given below :-



- Since drain terminal is kept floating, no current will be passing through the channel i.e. $I_D = 0$

A parallel plate capacitor is created at the gate region with polycrystalline silicon plate and induced N-channel as the two plates of capacitor and SiO_2 as the dielectric.

The MOSFET Now working as a capacitor.

For mos capacitor :→

The oxide capacitance per unit cross sectional Area is (C_{ox}).

$$\Rightarrow \boxed{C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}} \quad F/m^2$$

ϵ_{ox} = permitivity in F/m.

$\epsilon_{ox} = \epsilon_0 \epsilon_{r(SiO_2)}$.

ϵ_0 = Absolute permitivity of free space.

$\epsilon_0 = 8.854 \times 10^{-12}$

ϵ_r = Relative permitivity of SiO_2.

$\epsilon_r = 3.9$.

$\epsilon_0 \epsilon_r = 8.854 \times 3.9 \times 10^{-12}$

$$\boxed{\epsilon_0 \epsilon_r = 3.45 \times 10^{-11} \; F/m}$$

$$\Rightarrow \boxed{C_{ox} = \frac{3.45 \times 10^{-11}}{t_{ox}} \; F/m^2}$$

Gate Capacitance (C_{gate})

$$\Rightarrow \boxed{C_{gate} = C_{ox} \cdot W \cdot L} \quad \text{Farad.}$$

W → width of gate plate

L → length of gate plate or channel

$\Rightarrow \boxed{W > L}$ in MOSFET.

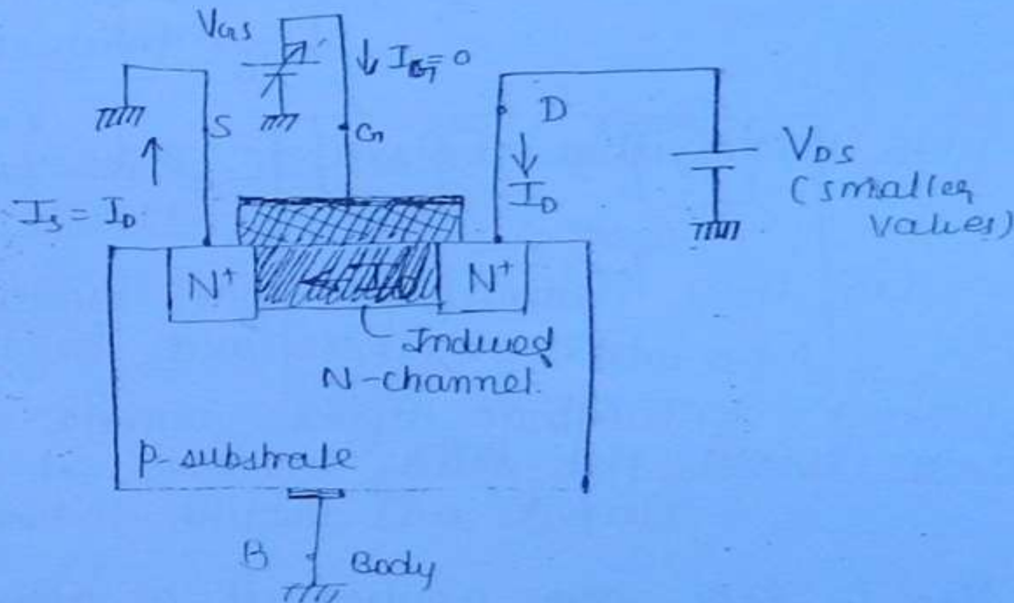
→ $W > L$

or

$\frac{W}{L} > 1 \Rightarrow$ Aspect Ratio.

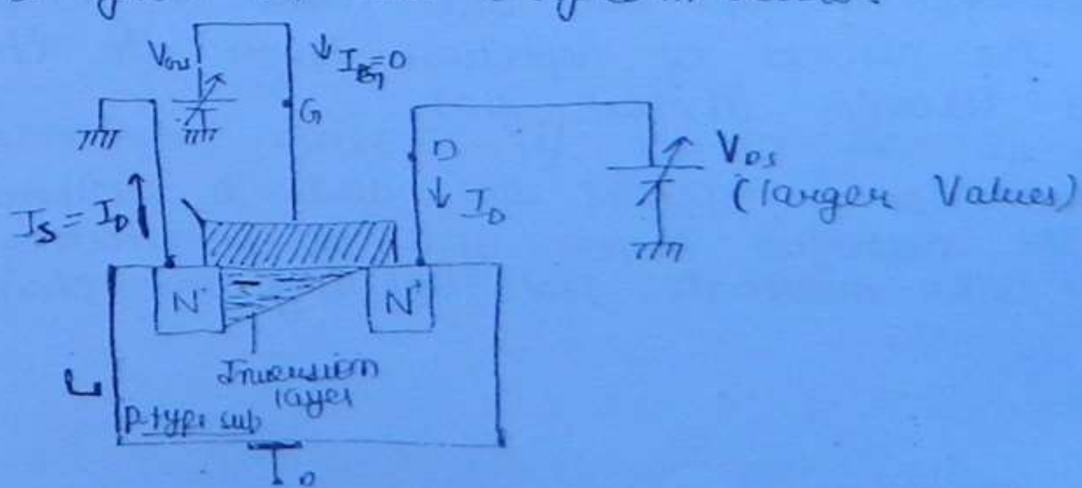
⇒ length of the gate plate is equal to the length of the channel.

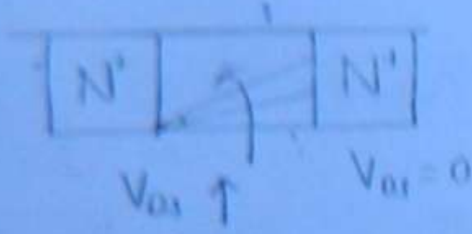
→ The drain current can pass through the MOSFET only when V_{DS} is applied.



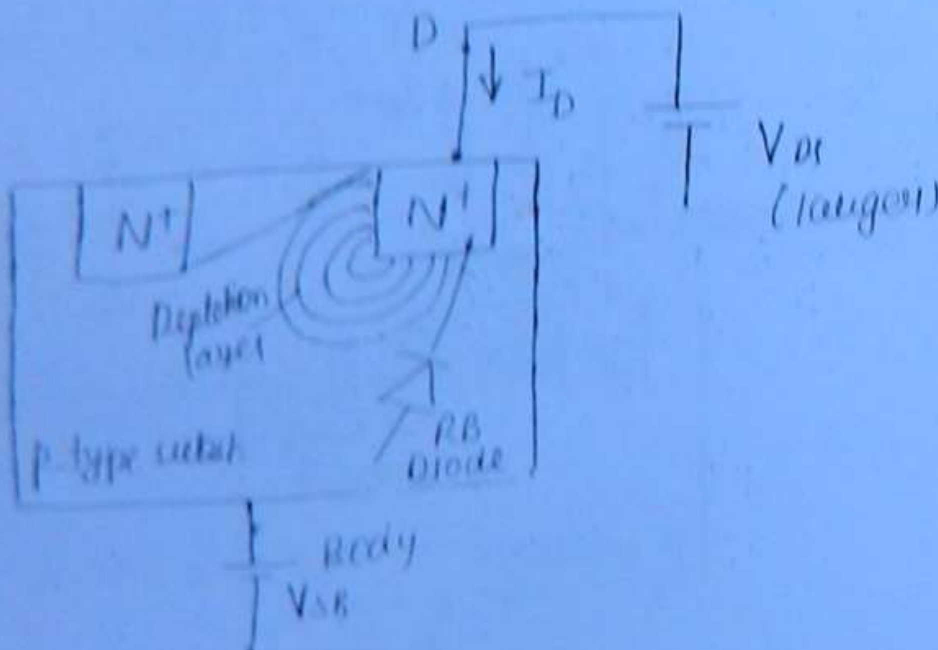
→ When smaller values of V_{DS} is applied the channel will remain almost flat as given in the above and drain current will pass into the channel.

→ When larger values of V_{DS} is applied, the channel gets tapered as given in the diagram below.





→ when V_{DS} is kept zero the channel remains flat
→ when V_{DS} is applied the increasing the channel get tappered.



→ when V_{DS} is kept zero applied it is appearing between drain and source and also between drain and body of the MOSFET.
The drain and body of MOSFET as a reverse biased diode.
→ when V_{DS} is kept zero the diode is unbiased and in the absence of depletion layer the channel will remain almost flat
→ when V_{DS} is applied the diode is reverse biased & the depletion layers will be penetrating more into the substrate and tapping the channel

→ When larger V_{DS} is applied there is a discontinuity in the channel and the channel will be broken but due to the larger E.F. intensity the drain current will remain almost constant.

→ The discontinuity of the channel can be avoided by connecting substrate voltage V_{SB} or body voltage

→ When V_{DS} is increasing the channel length decreases and this process where the length of the channel can be alter by varying V_{DS} is called channel length modulation

→ ★ Channel length modulation will occur only in E-only MOSFET.

→ The channel length modulation will not exist in depletion MOSFET and JFET

→ ★ Due to channel length modulation E only MOSFET cannot be operated with self biased arrangement or potential divider bias circuit

→ In N-channel enhancement MOSFET :-

① channel potential increases from source to drain

② Inversion charge decreases from source to drain

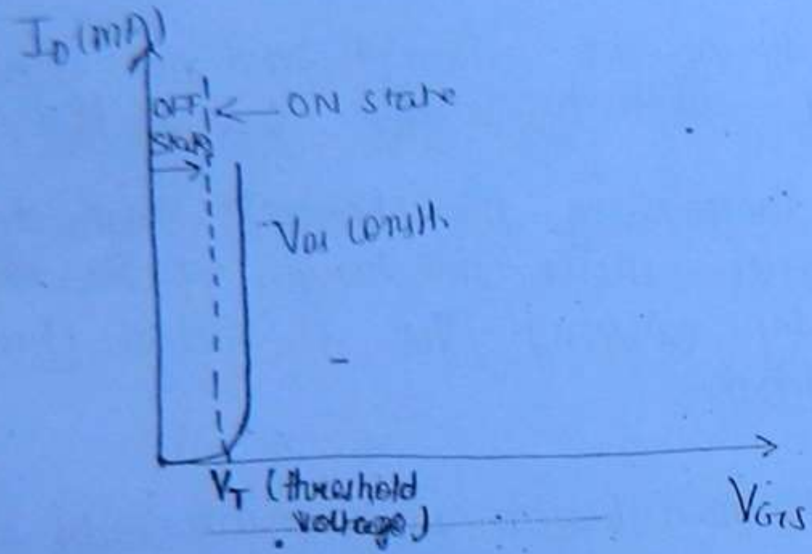
→ In enhancement MOSFET when V_{GS} is kept zero and V_{DS} is existing then channel will disappear

$\therefore I_D = 0$

Or

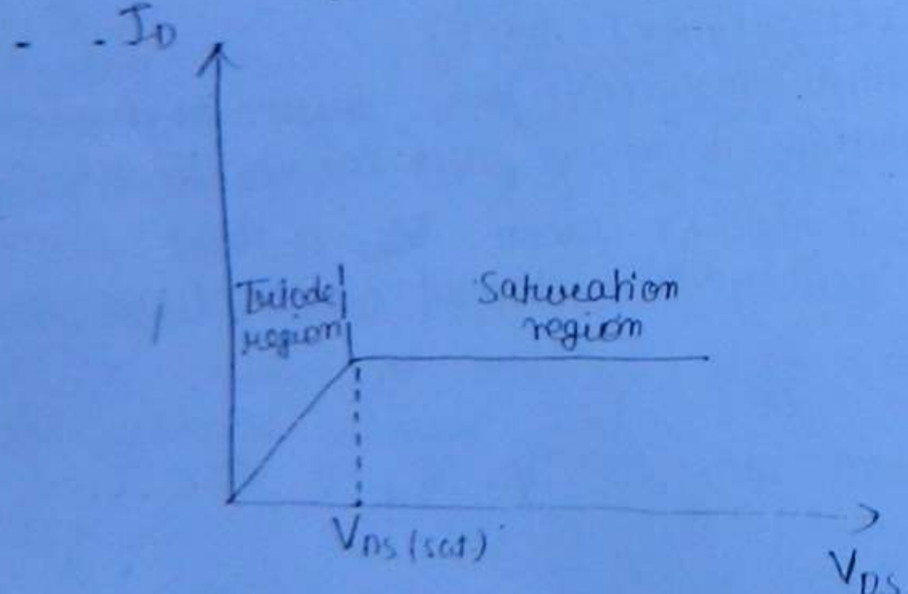
In enhancement MOSFET if $V_{GS} = 0$ then $I_D = 0$

Transfer characteristics for n-channel E-only MOSFET



- if $V_{GS} < V_T$, MOST is OFF state
- if $V_{GS} \geq V_T$, MOST is ON i.e. SC

Drain characteristics of N channel E-only MOST.



$$\Rightarrow \boxed{V_{DS(sat)} = (V_{GS} - V_T)}$$

Triode Region

Also called ohmic region or linear region or non-saturation region.

$$\therefore \forall \left\{ \begin{array}{c} V_{DS} < V_{DS(sat)} \\ \text{or} \\ V_{DS} < (V_{GS} - V_T) \end{array} \right\}$$

Saturation Region (Pentode Region) or pinch-off region :-

$$\forall \left\{ \begin{array}{c} V_{DS} \geq V_{DS(sat)} \\ \text{or} \\ V_{DS} \geq (V_{GS} - V_T) \end{array} \right\}$$

Equation for drain current in the saturation region of E-only MOSFET.

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_T} \right]^2 \text{ Amp}$$

$$\left[\because V_{GS} >> V_T \right]$$

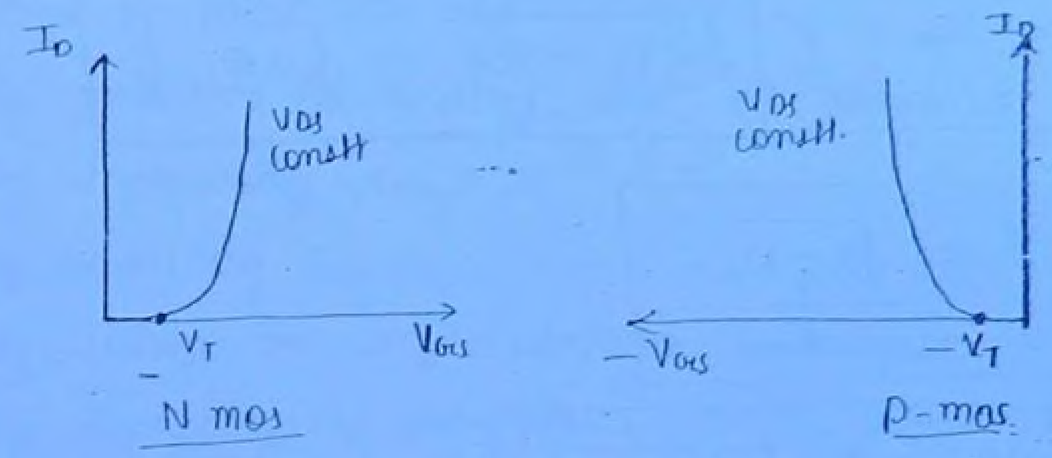
→ The above equation indicates in the E-only MOST I_D increases as a parabolic variation with V_{GS}.

Comparison between Depletion MOSFET & E-only MOST.

Depletion MOSFET	Enhancement MOST
1) Preexisting channel is available.	1) No preexisting channel and channel has to be created by applying proper V_{GS}.
2) Diffused channel	2) Induced channel.
3) Suitable to operate in Depletion and enhancement mode.	3) Suitable only for enhancement mode
4) When $V_{GS} = 0$, $I_D = I_{DSS}$	4) When $V_{GS} = 0$, $I_D = 0$.
5) No channel length modulation	5) Channel length modulation exist
6) Continuous channel	6) Channel is discontinued.
7) Comparatively larger in size and expensive due to provision of Al plate.	7) Comparatively smaller in size, economical and better performance due to replacement of Al plates by polycrystalline Si material
8) Can be designed in self biased arrangement	8) Cannot be designed in self biased arrangement

THRESHOLD VOLTAGE (V_T or V_t or V_{th}) :→

→ It is also called gate to source threshold voltage denoted by V_{GST}.



→ Threshold voltage is defined as the minimum V_{GS} where the MOST enters into ON state.

→ For N-mos threshold voltage is +ve.

→ For pmos V_{th} is -ve.

→ V_T → 0.5V to 3V. [typ value 1V]

→ For better performance of MOST V_T must be smaller

→ V_T can be graphically obtained from the transfer characteristics of MOST.

→ V_{th} will appear only in E-only MOST.

→ Advantages of V_{th} smaller :→

① It ENABLE the device to operate with smaller supply voltages

② It increases the compatability of device

③ Reduces switching time device so that MOST become faster in operation

Equation for V_{th} :-

N channel enhancement most V_{th} is given by :-

$$\Rightarrow \boxed{V_{th} = V_{to} + \gamma\left[\sqrt{2\varphi_f + V_{SB}} - \sqrt{2\varphi_f}\right]}$$

$$\Rightarrow \boxed{\gamma = \frac{\sqrt{2qN_A\epsilon}}{C_{ox}}}$$

$$\Rightarrow \boxed{\gamma = \frac{t_{ox}\sqrt{2qN_A\epsilon}}{3.45\times10^{-11}}}$$

→ γ is called fabrication process parameter

→ φ_f physical parameter or fermi voltage

→ V_{SB} substrate voltage or Body voltage

→ N_A Acceptor concⁿ or doping concⁿ of p-type substrate in N channel most.

→ V_{to} is threshold voltage of most when substrate voltage is kept zero ($V_{SB}=0$)

→ V_{th} of most can be increased by increasing V_{SB}.

→ Suppose if there is a small variation in substrate voltage this will cause small variation in V_t in this result a small variation in I_D it follows that V_{SB} controls the gate current Hence Body will be acting as the II^nd gate in the MOSFET this property is called "Body effect"

Procedure to Reduce V_T :→

→ The V_{th} of MOST can be reduced by using anyone of the following methods (it should be done only at time of fabricating the device)

→ By reducing the doping concⁿ of substrate material.

→ By increasing C_{ox}

→ By reducing t_{ox}.

→ By using ion implantation technique.

→ By replacing the Al. plates with polycrystalline Si material (Al is a metal with larger contact potential while polycrystalline Si is oxide material with very low contact potential becoz of smaller contact potential the V_{th} of MOST can be reduced)

→ Polycrystalline Si is also called poly Si.

→ Alternative material for polycrystalline Si material is Si Nitride.

→ In modern MOST gate material polycrystalline Si

Equations For Nmos Transistor :→

(1) Over drive voltage :→ V_{ov}

$$\Rightarrow \boxed{V_{ov} \equiv V_{DS(sat)} \text{ or } V_{ov} \equiv (V_{GS} - V_T)}$$

(2) Operation in Triode Region :→

condition :- $V_{DS} < V_{DS(sat)}$

$\Rightarrow V_{DS} < (V_{GS} - V_T)$

$$i_d = \mu_n C_{ox} \frac{W}{L} \left\{ (V_{gs} - V_T) V_{ds} - \frac{V_{ds}^2}{2} \right\}$$

Triode regions occurs for smaller value of V_{ds}

∴ neglecting $V_{ds}^2/2$

$$i_d = \mu_n C_{ox} \frac{W}{L} \left\{ (V_{gs} - V_T) V_{ds} \right\}$$

$$\Rightarrow \boxed{i_d = \mu_n C_{ox} \frac{W}{L} \left[(V_{gs} - V_T) V_{ds} \right]}$$

Let $\mu_n C_{ox} = K_n$ → Process Transconductance parameter in A/V^2

$$\Rightarrow \boxed{i_d = K_n \frac{W}{L} (V_{gs} - V_T) V_{ds}]}$$

$$\Rightarrow K_n \frac{W}{L} = K_n' \rightarrow \text{constant in } A/V^2$$

$$\Rightarrow \boxed{i_d = K_n' \left[(V_{gs} - V_T) V_{ds} \right]}$$

⇒ The equation is a I^{st} order equation and the curve represent a linear variation

Drain to source resistance given by

$$\Rightarrow \boxed{r_{ds} = \frac{V_{ds}}{i_d}}$$

$$\Rightarrow \boxed{r_{ds} = \frac{1}{K_n' [V_{gs} - V_T]}} \ \Omega$$

$$\Rightarrow \boxed{r_{ds} = \frac{1}{\mu_n C_{ox} \frac{W}{L} \left[(V_{gs} - V_T) \right]}} \ \Omega$$

⇒ This indicates that in the ohmic region or triode region FET will be working as voltage variable resistor by varying V_{GS}

In the triode region, the transconductance of FET

$$g_m = \left. \frac{\partial i_d}{\partial V_{gs}} \right|_{V_{ds}}$$

$$i_d = k_n' [V_{gs} - V_T] V_{ds}$$

$$\frac{\partial i_d}{\partial V_{gs}} = k_n' V_{ds}$$

$$\Rightarrow \boxed{g_m = k_n' V_{ds}}$$

$$\Rightarrow \boxed{g_m = \mu_n C_{ox} \frac{W}{L} V_{ds}}$$

(iii) <u>Operation in Saturation region</u> :-

cond^n — $V_{DS} \geq V_{DS(sat)}$

$\Rightarrow V_{DS} \geq (V_{GS} - V_T)$

$$i_d = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_T)^2$$

$$i_d = \frac{1}{2} k_n \frac{W}{L} (V_{gs} - V_T)^2$$

$$\Rightarrow \boxed{i_d = K (V_{gs} - V_T)^2}$$

Let $\frac{1}{2} k_n \frac{W}{L} = K$ → A/V^2

IInd order equation and this indicates i_d increases as a parabolic variation with V_{GS}

→ The transconductance in saturation region

$$g_m = \left.\frac{\partial i_d}{\partial V_{GS}}\right|_{V_{DS}}$$

$$i_d = K\,(V_{gs} - V_T)^2$$

$$\frac{\partial i_d}{\partial V_{gs}} = 2K\,[V_{gs} - V_T]$$

$$\Rightarrow \boxed{g_m = 2K\,[V_{gs} - V_T]}\ \mho$$

$$\Rightarrow \boxed{g_m = \mu_n C_{ox} \frac{W}{L}\,[V_{gs} - V_T]}\ \mho$$

$$r_{ds} = \frac{1}{K_p' [V_{gs} - V_T]}$$

$$\Rightarrow \boxed{g_m = K_p' V_{ds}}$$

(iii) Operation in Saturation Region :→

cond^n $\left\{ \begin{array}{l} V_{DS} \leq V_{DS(sat)} \\ V_{DS} \leq (V_{GS} - V_T) \end{array} \right\}$

$$i_d = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} \{ V_{gs} - V_T \}^2$$

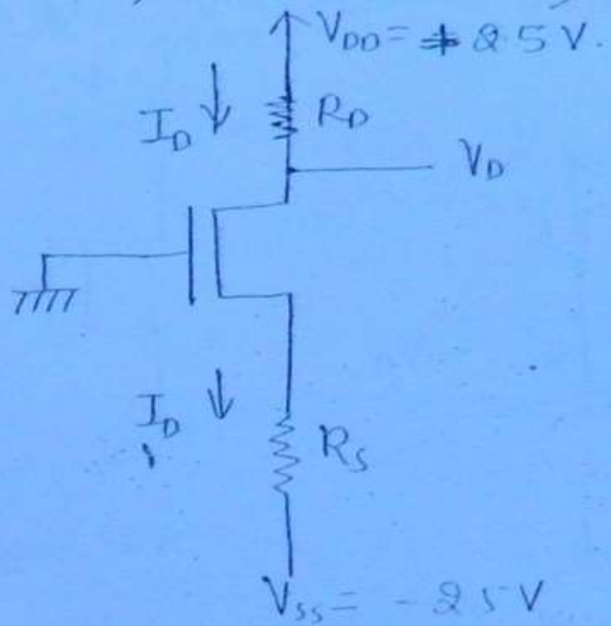
$$= \frac{1}{2} k_p \frac{W}{L} (V_{gs} - V_T)^2$$

$\frac{1}{2} k_p \frac{W}{L} = K \Rightarrow$ constt. in A/V^2

$$\Rightarrow * \boxed{i_d = K (V_{gs} - V_T)^2}$$

$$\Rightarrow * \boxed{g_m = 2K [V_{gs} - V_T]}$$

Prob Design the circuit shown below so that Tr. operate at $i_d = 0.4\,mA$ and $V_d = 0.5\,V$ the nmos transistor has $V_T = 0.7\,V$
$\mu_n C_{ox} = 100\,\mu A/V^2$, $L = 1\,\mu m$, $W = 32\,\mu m$



Soln Since gate is grounded $V_g = 0$
$V_D > V_G$ the mos is in sat. Region

$$i_d = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_T)^2$$

$$0.4\times10^{-3} = \frac{1}{2}\times100\times10^{-6}\times32\,(V_{gs} - 0.7)^2$$

$$0.4\times10^{-3} = 10^{-4}\times16\,(V_{gs} - 0.7)^2$$

$$4\times10^{-4} = 16\times10^{-4}(V_{gs} - 0.7)^2$$

$$R_D = \frac{V_{DD} - V_D}{I_D}$$

(5 KΩ)

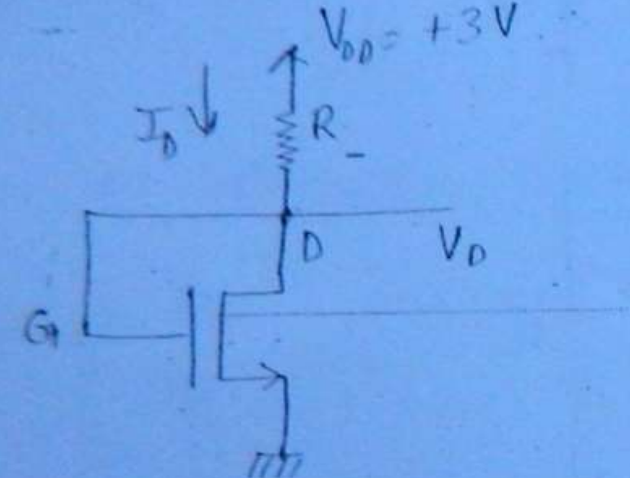
$$2 = 4\,(V_{gs} - 0.7)$$

$$2 = 4V_{gs} - 0.7$$

$$4V_{gs} = 1.3 \Rightarrow V_{gs} = \frac{1.\ }{4} = 1.2$$

$$V_G = V_{GS} + I_D R_S + V_{SS} = 1.2 + 0.4\times10^{-3}(R_S) - 2.5 = 1$$

Prob: Design the circuit given to obtain a current $I_D = 80\mu A$ find the value require for R & D.C voltage V_D. The nmos Tr. has $V_T = 0.6V$, $\mu_n C_{ox} = 200\mu A/V^2$, $L = 0.8\mu m$, $W = 4\mu m$?



Soln

since G & D are SC

$V_{GS} = V_{DS}$

It is work as switch.

$$i_d = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)^2$$

$$80 \times 10^{-6} = \frac{1}{2} \times 200 \times \frac{4}{0.8}(V_{GS} - 0.6)^2$$

$$8 = \frac{10 \times 4}{0.8}(V_{GS} - 0.6)^2$$

$$4 = 25(V_{GS} - 0.6)^2$$

$$2 = 5(V_{GS} - 0.6)$$

$$2 = 5V_{GS} - 3 \Rightarrow 5V_{GS} = 5$$

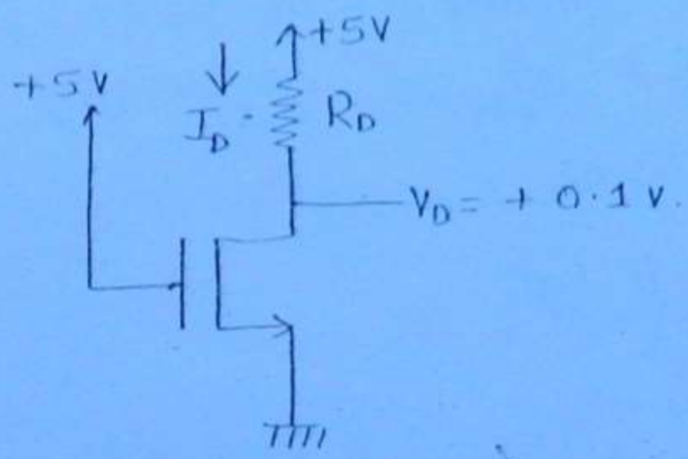
$$V_{GS} = 1V$$

$$R = \frac{3 - 1}{80 \times 10^{-6}}$$

$$R = 25k\Omega$$

Part Design the circuit given to establish a drain voltage $V_D = 0.1\,V$ what is the effective resistance between drain & source at this operating point.

$V_T = 1\,V$, $K_n \frac{W}{L} = 1\,mA/V^2$?



Soln

$V_{GS} = 5\,V$

$V_{DS} = V_D = 0.1\,V$

$V_G > V_D$ most is in Triode

$$i_d = \mu_n C_{ox} \frac{W}{L} \left[(V_{gs} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$i_d = 1m \left[(5 - 1)0.1 - \frac{(0.1)^2}{2} \right]$$

$i_d = 0.395\,mA$

$$R_D = \frac{5 - 0.1}{0.395} = 12.4\,K\Omega$$

$$r_{ds} = \frac{V_{DS}}{I_D} = \frac{0.1}{0.395 \times 10^{-3}} = 253\,\Omega$$

Consider a p-channel enhancement mode mosfet with $K_p = 40 \mu A/V^2$ the device has following observations :-

$I_{D1} = 0.225\ mA$ at $V_{SG1} = V_{SD1} = 3V$

$I_{D2} = 1.4\ mA$ at $V_{SG2} = V_{SD2} = 4V$

find V_{TP} & Aspect Ratio.

Sol: $V_{SG} \equiv V_{SD}$ most is sat.

$i_d = K[V_{GS} - V_T]^2$

$i_d = K[V_{SG} - |V_{TP}|]^2$ —

$$\frac{I_{D1}}{I_{D2}} = \frac{[V_{SG1} - |V_{TP}|]^2}{[V_{SG2} - |V_{TP}|]^2}$$

$$\frac{0.225}{1.4} = \frac{[3 - |V_{TP}|]^2}{[4 - |V_{TP}|]^2}$$

$|V_{TP}| = 2.33\ V \Rightarrow V_{TP} = -2.33\ V$

Aspect Ratio

$I_{D1} = \frac{W}{L} \frac{K'}{2} [V_{SG1} - |V_{TP}|]^2 = 0.225$

$\rightarrow \frac{W}{L} = 25$

Prob An ideal n channel MOSFET as the following specification:

$W = 30\mu m$, $L = 2\mu m$, $\mu_n = 450\ cm^2/V sec$

$t_{ox} = 350 Å$, $V_{TN} = 0.8V$ if Tr. is operating in sat. region if $V_{GS} = 4V$

Soln

$$g_m = K' V_{ds}$$

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) \; 25$$

$$= \mu_n \left[\frac{3.45 \times 10^{-11}}{350 \times 10^{-10}}\right] \frac{W}{L} (V_{GS} - V_T)$$

$$= 0.045 \left[\frac{3.45 \times 10^{-11}}{350 \times 10^{-10}}\right] \left(\frac{30}{2}\right) [4 - 0.8]$$

$$g_m = 2.13\ mS$$